Semiconductors Material & Devices Lab

Manual

M.Sc Electronics (Semester 1)

Guru Ghasidas Vishwavidyalaya
(A central University)
Koni, Bilaspur, C.G. India
495009

List of Experiments

1. Measurement of resistivity of sample at various temperatures by four probe method.
2. To calculate the energy band gap of given semiconductor sample.
3. To study the Hall Effect: determine the Hall coefficient, type of semiconductor and carrier concentration in the given semiconductor sample.
4. I-V characteristics measurements of a p-n diode/Schottky diode calculate its device Parameters.
5. To study the performance of solar cell.
6. To study the characteristics of JFET and its application as switch.
7. To study the characteristics of MOSFET and its application

Four Probe Method

Aim:

Study the temperature dependence of resistivity of a semiconductor (Four probe method) and to determine band gap of experimental material (Ge).

Apparatus Required:

Four probe apparatus, sample (a Ge crystal in form of a chip), oven, thermometer (260^o) constant power supply, oven power supply, panel meters for measurement of current and voltage.

Formula Used : Resistivity of a semiconductor is

$$\rho = A \exp\left(\frac{E_g}{2k_BT}\right)$$

Where E_g is Band Gap in eV

k_B is Boltzman constant =8.617*10^{-5} eVK^{-1}

and T is absolute Temperature

Principle :

Ohm's law: If physical conditions (like temperature, mechanical stress) remains unchanged, then potential difference across two ends of a conductor is proportional to current flowing through it

$$V \propto I$$

$$V = IR$$

The constant of proportionality, R, is called resistance of the conductor.

Resistivity: At a constant temperature, the resistance, R, of a conductor is (i) proportional to its length and (ii) inversely proportional to its area of cross-section,

$$R = \rho \frac{L}{A}$$

The constant of proportionality, ρ , is called resistivity of material of the conductor. Resistivity of a material is equal to the resistance offered by a wire of this material of unit length and unit cross-sectional area. Unit of resistance is ohm (Ω), and unit of resistivity is ohm-meter (Ω-m)

Four probe method: The 4-point probe set up (Fig.I & Fig.II) consists of four equally spaced tungsten metal tips with finite radius. Each tip is supported by springs on the end to minimize sample damage during probing. The four metal tips are part of an auto-mechanical stage which travels up and down during measurements. A high impedance current source is used to supply current through the outer two probes, a voltmeter measures the voltage across the inner two probes to determine the sample resistivity. Typical probe spacing ~ 2 mm. These inner probes draw no current because of the high input impedance voltmeter in the circuit. Thus unwanted voltage drop (I R drop) at point B and point C caused by contact resistance between probes and the sample is eliminated from the potential measurements. Since these

contact resistances are very sensitive to pressure and to surface condition (such as oxidation of either surface).

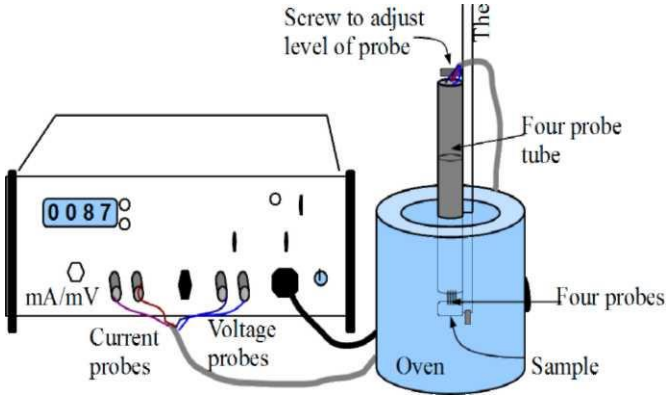


Fig.I Schematic diagram of a Four Probe

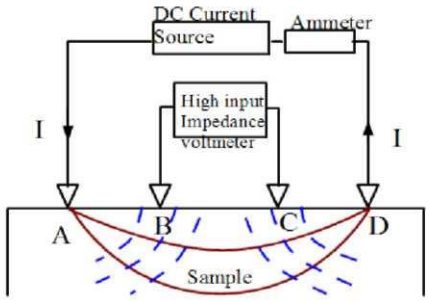


Fig.II

Resistivity of Germanium (semiconductor) crystals or slices:

In order to use this four probe method in germanium crystals or slices it is necessary to assume that: The resistivity of the material is uniform in the area of measurement and a non conducting boundary is produced when the surface of the crystal is in contact with an insulator. The derivation of equations given below are involved. For each case it is assumed that the probes are equally spaced (spacing =s).

Case I: Resistivity Measurements on a Large Sample:

We assume that the metal tip is infinitesimal and sample are semi infinite in lateral dimensions. For bulk samples where the sample thickness, W >> S , the probe spacing, we assume a spherical protrusion of current emanating from the outer probe tips. The resistivity is computed to be

$$\rho_o = \left(\frac{V}{I}\right) * 2\pi s$$

where

V = floating potential difference between the inner probes, unit: volt

I =current through the outer pair of probes, unit: ampere

s = spacing between point probes, unit: meter

ρ_0 = resistivity, unit: ohm meter

Case II: Resistivity Measurements on a Thin Slice-Nonconducting Bottom Surface:

For the case of a nonconducting bottom on a slice the resistivity is computed from

$$\rho = \frac{\rho_0}{G_7(\frac{W}{S})}$$

$G_7\left(\frac{W}{S}\right)$ can be calculated from graph (1) or from Table (1) given below or using formula

$$G_7(w/s) = \frac{2s}{w}\log_e 2$$

Table 1

S.No.	W/S	G_7(W/S)	S.No.	W/S	G_7(W/S)
1.	0.100	13.863	6.	1.000	1.504
2.	0.141	9.704	7.	1.414	1.223
3.	0.200	9.631	8.	2.000	1.094
4.	0.330	4.159	9.	3.333	1.0228
5.	0.500	2.780	10.	5.000	1.0070

Temperature dependence of resistivity of a semiconductor:

Intrinsic semi-conduction The process in which thermally or optically excited electrons contribute to the conduction is called intrinsic semi-conduction. In the absence of photonic excitation, intrinsic semi-conduction takes place at temperatures above 0 K as sufficient thermal agitation is required to transfer electrons from the valence band to the conduction band. Conductivity for intrinsic semi-conduction. The total electrical conductivity is the sum of the conductivities of the valence and conduction band carriers, which are holes and electrons, respectively. It can be expressed as

$$\sigma = e(n_e\mu_e + n_h\mu_h) \quad (1)$$

where n_e , μ_e are the electron's concentration and mobility,
and n_h , μ_h are the hole's concentration and mobility, respectively.
Drift mobility determines the average drift velocity in the presence of an applied external field. It also depends on the temperature. The mobility is a quantity that directly relates the drift velocity v_d of charge carriers to the applied electric field E across the material, i.e.,

$$\mu = v_d / E \quad \ldots\ldots\ldots\ldots \quad (2)$$

In the intrinsic region the number of electrons is equal to the number of holes, $n_e=n_h=n_i$, so Equation (1) implies that,

$$\sigma = e n_i (\mu_e + \mu_h) \quad (3)$$

The electron density (electrons/volume) in the conduction band is obtained by integrating (density of states x probability of occupancy of states) from the bottom to top of the conduction band. The detailed calculations reveal that

$$n_i = NT^{\frac{3}{2}} \exp\left(-\frac{E_g}{2k_BT}\right) \quad (4)$$

Where N is a contant substituting n_i in eq (3)

$$\sigma = e(\mu_e + \mu_h) NT^{\frac{3}{2}} \exp\left(-\frac{E_g}{2k_BT}\right) \quad (5)$$

This shows that conductivity depends on temperature it decreases exponentially with decrease in temperature.

Temperature dependence of resistivity

$$\rho = \frac{\exp\left(\frac{E_g}{2k_BT}\right)}{e(\mu_e + \mu_h) NT^{\frac{3}{2}}} \quad (6)$$

Or,

$$\rho = A \exp\left(\frac{E_g}{2k_BT}\right) \quad (7)$$

Where A is a constant Taking Log

$$\ln \rho = lnA + \frac{E_g}{2k_BT} \quad (8)$$

or

$$\log \rho = C + \frac{1}{2.3026} * \frac{E_g}{2k_BT} \quad (9)$$

where *C* is a constant . Rewriting eq (9)

$$\log \rho = C + \frac{1}{2.3026*10^3} * \left(\frac{E_g}{2k_B}\right)\left(\frac{1000}{T}\right).$$

Therefore, if a graph is plotted $\log \rho$ vs $\left(\frac{1000}{T}\right)$ it should be a straight line and band gap E_g can be determined from its slope as follows :

1. Slope = $\frac{AC}{BC} = \frac{1}{2.3026*10^3} * \frac{E_g}{2k_B}$,
2. Band gap $\mathbf{E_g = 2.3026*10^3*2*k_B*slope}$ eV, (Take Boltzman constant $k_B = 8.617*10^{-5}$ eVK^{-1}).

Method :

(1) The setting of 4-point probes on the semiconductor chip is a delicate process. So first understand well the working of the apparatus. The semiconductor chip and probe set is costly.

(2) Note the values of probe spacing (S) and the thickness (W) of the semiconductor chip. Note the type of semiconductor (germanium or something else).

(3) Make the circuit as shown in Fig.1. Put the sample in the oven (normally already placed by lab instructor) at room temperature.

(4) Pass a milliampere range current (say 5 mA) in the sample using constant current power supply.

(5) The reading of the current through the sample is measured using milliammeter provided for this purpose. The voltage is measured by a high impedance milli voltmeter connected to the inner probes. The readings can be taken alternately on digital meter provided for this purpose.

(6) Note temperature of sample (oven) using thermometer inserted in the oven for this purpose.
(7) The oven temperature is increased a little, and its temperature noted after reaching steady state. Again the constant current reading (advised to be kept the same) and the corresponding voltage readings are taken.

(8) Repeat the procedure for different temperatures. Note the data in the observation table.

(9) For each temperature, calculate the resistivity by using the relation.

$$\rho = \frac{\rho_0}{G_7(\frac{W}{S})} = \left(\frac{V}{I}\right)\left(\frac{2\pi S}{G_7\left(\frac{W}{S}\right)}\right)$$

(10) Compute $log\ \rho$ and $10^3 / T$ and write it in the observation table.

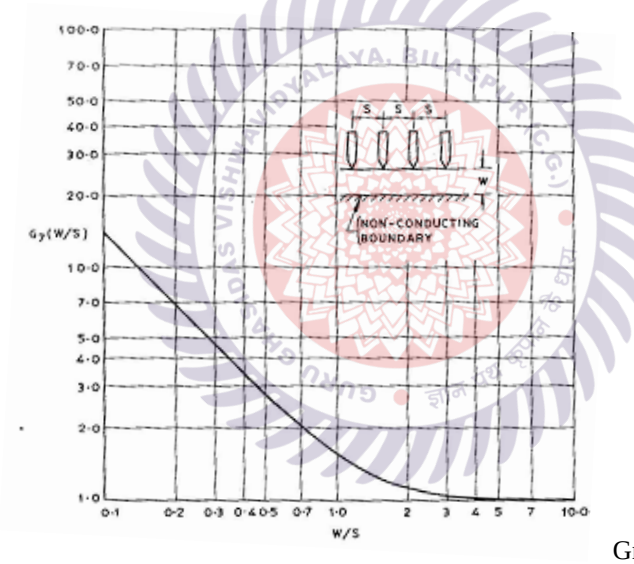
(11) Plot a graph between $log\ \rho$ and $10^3 / T$. It is a straight line. Find its slope.

(12) Calculate the band gap using formula

$$\mathbf{E_g = 2.3026 * 10^3 * 2 * k_B * slope}\ \text{eV}$$

Use Boltzman constant $k_B = 8.617 * 10^{-5}$ eVK^{-1}

($k_B = 1.3806 * 10^{(-23)}$ JK^{-1} and $1eV = 1.6 * 10^{-19}$ J)



Graph 1

Observations:

1. Semiconductor chip material = Germanium
2. Spacing (distance) between the probes, s = 2.0 mm =..... m.
3. Thickness of the sample, w =0.5 mm = ... m.

Table : Voltage across the inner probes for a constant current at different sample temperatures

Current (I) = ……mA

S.No.	Temperature T (K)	Voltage across inner probes (mV)	$\frac{1000}{T}\ K^{-1}$ (calculated)	Resistivity ρ $\rho = \left(\frac{V}{I}\right)\left(\frac{2\pi S}{G_7\left(\frac{W}{S}\right)}\right)$ (ohm-cm)	Log ρ (calculated)
1					
2					
3					
..					
..					

Calculations:

1 For the given sample $\left(\frac{W}{S}\right)$= ……..

2. The correction factor G_7 (w /s) =(from table 1 or graph 1) or calculate G_7(W/S) as follows:

$$G_7 \text{ (w /s)} = \frac{2 * s}{w} \ln 2$$

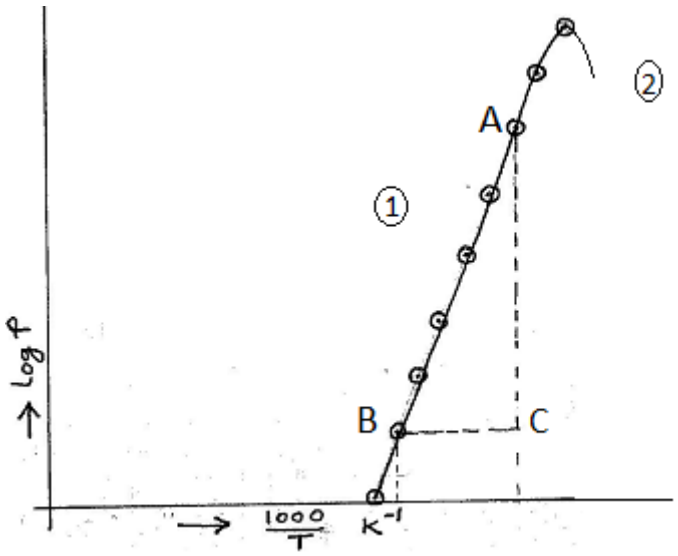
3. Calculation of T (K^{-1}) , ρ (ohm-m) and $log\rho$

$$\rho = \frac{\rho_0}{G_7\left(\frac{W}{S}\right)} = \left(\frac{V}{I}\right)\left(\frac{2\pi S}{G_7\left(\frac{W}{S}\right)}\right)$$

4. The graph between $\frac{1000}{T}$ and log ρ is plotted as shown in graph (2)

5. Slope of the straight line is $\frac{AC}{BC}$

6. Energy band gap $E_g = 2.3026 * 2 * k_B * \text{slope} * 10^3$(in eV)



Graph 2 Variation of logρ with $\frac{1000}{T}$

Explanation of Graph-2

The resistivity of a Germanium crystal as a function of inverse temperature. For this sample when T < T' ^{0}K i.e. region (2), conduction is mainly due to the impurity carriers (extrinsic region). For T > T' ^{0}K conduction is due to electrons transferred to the conduction band and the corresponding holes created in the valence band (this is the intrinsic region).

Result:

1. The temperature dependence of the resistivity of semiconductor (germanium) chip is as shown in the graph (2) . The resistivity decreases exponentially with the increase in *T.* That is as at low temperatures resistivity is more and at high temperatures the resistivity is less.

2. The energy band gap for the given semiconductor (germanium) is = ……eV.

Precautions:

1. The surface of the semiconductor should be flat.
2. All the four probes should be collinear.
3. The adjustment of 4-point probes should be done gently, as the semiconductor chip is brittle.
4. The voltage should be measured using inner probes only using a high impedance millivoltmeter.
5. Temperature of the oven should not exceed the limits set by manufacturer of the probes and chip.

ENERGY GAP OF SEMICONDUCTOR

Aim: To determine the Energy gap of the semiconductor(Thermister)

Apparatus: Thermister, power supply, resistor, voltmeter and milli-ammeter.

Formula:

$$E_g = \frac{2.303 \times 2K \times S}{1.601 \times 10^{-19}} \text{ eV}$$

where, E_g= Energy gap of given semiconductor, eV

K= Boltzman's constant, 1.38×10^{-23} Jk^{-1}
S= Slope of the graph

Procedure: An Ohmmeter is connected across the thermistor (Red to Red & Black to Black) and the resistance of the thermistor at the room temperature is noted. Then the thermistor is immersed in oil bath and heated to a temperature of 95°C. Then while cooling the resistance of the thermistor is noted from Ohmmeter for different temperatures starting from 90°C till 50°C for every 5°C reduction in temperature. The readings are tabulated. A plot of Log R versus 1/T is made. Slope(S)of the curve is determined. The energy gap of the given semiconductor is calculated using the formula.

$$\text{Eg} = \frac{2.303 \times 2K \times S}{1.601 \times 10^{-19}} \text{ eV}$$

[**Note:** Thermistors are made of semiconductors. The variation of resistance (R) of a thermister with temperature (T) is given by

$R = R_0 e^{+\frac{Eg}{2KT}}$ Taking Log_{10} on both the sides $\left(R = R_0 \exp\left[+\frac{E_g}{2kT}\right]\right.$

$\text{Log } R = \text{Log } R_0 + \frac{Eg}{2KT} \text{Log} e^{\frac{1}{T}}$ $\ln R = \ln R_0 + \frac{E_g}{2kT}$

A plot of Log R versus 1/T must be a straight line with slope.

$$S = \frac{Eg}{2K} \text{ Log e}$$

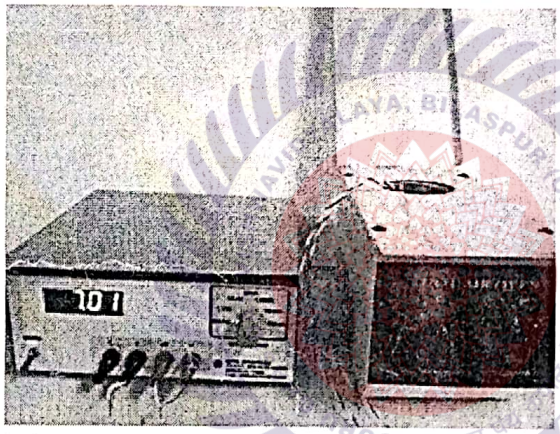
$$E_g = \frac{2KS}{Loge} = 2.303 \times 2 \text{ KS J}$$

$$E_g = \frac{2KS}{Loge} = \frac{2.303 \times 2KS}{1.601 \times 10^{-19}} \text{ eV}$$

Procedure:

1. Connect the thermister to the main unit (Red connector to red connector and black connector to black connector). Keep the selector knob at suitable range.

2. Place the thermistor into the beaker having silicon oil and put it into the Hot Air Oven with thermometer. Keep Energy Control knob of oven at 80.

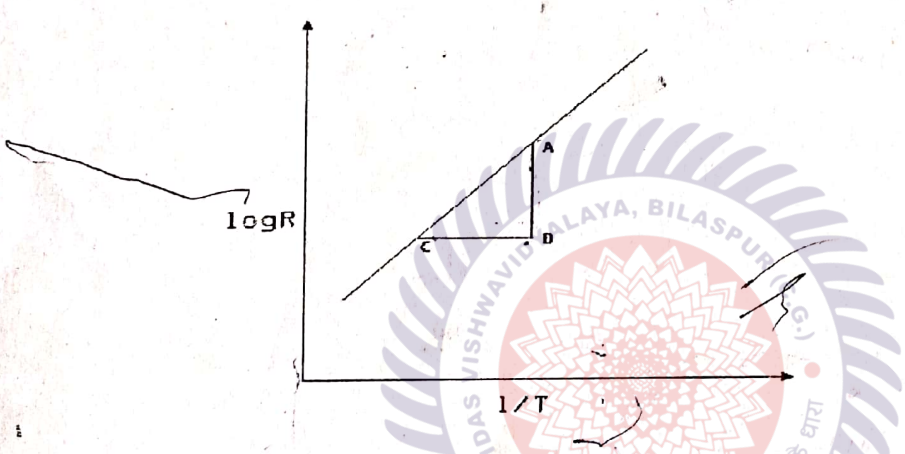


3. Switch ON the heater and heat it upto 90 deg C and switch off the heater.

4. Now allow the temperature to cool down and tabulate the resistance at different temperature as shown below:

Sl No	Temp(°C)	Temp (K)	Resistance (in Ω)	Log R	1/T (K^{-1})
1	90				
2	85				
3	80				
4	75				
5	70				
6	65				
7	60				

5. Plot the Graph between Log R and 1/T. It will be a straight line. Calculate the slope from the graph



Boltzman Constant k=1.38×10^{-23} JK^{-1}

6. Calculate energy gap using relation

$$E_g = \frac{2.303 \times 2K \times S}{1.601 \times 10^{-19}} \text{ eV}$$

Result: Energy gap of the material given semiconductor is, Eg =……eV

DETERMINATION OF HALL COEFFICIENT BY USING HALL APPARATUS

Requisites

Hall Probe (Ge crystal & InAs Crystal) Hall effect setup (Digital)

Electromagnet Constant current power supply.

Digital Gaussmeter.

Theory

When an electrical current passes through a sample placed in a magnetic field, a voltage develops across the sample in a direction perpendicular to both the current and the magnetic field. This is known as Hall effect. The basic experimental setup for study of Hall effect is shown in Fig. 9.1. A rectangular slab of a semiconducting sample with its *width* (*w*) along *y*-direction and *thickness* (*d*) along *z*-direction is placed in a magnetic field of strength *B* directed along the *z*-direction. Now an electric current, I_H is made to pass through the sample along its length by maintaining a potential difference along *x*-direction. The corresponding current density is,

$$J_x = \frac{I_H}{wd} \tag{1}$$

Suppose that the charge carriers are positive, each having charge $+q$, and are moving along $+x$ direction with velocity $\vec{v}$. Then the Lorentz force experienced by the carriers due to themagnetic field is,

$$\vec{F}_B = q(\vec{v}X\vec{B}) = -(qvB)\hat{y} \tag{2}$$

This force $\vec{F}_B$along $-\hat{y}$ direction deflects the positive charge carriers towards the *bottom surface* of the sample. This makes the *bottom surface* positively charged while leaving the *top surface* negatively charged. This

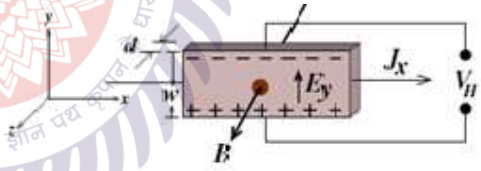


Fig. 9.1

accumulation of charges near the bottom and top surfaces of the sample leads to the development of a transverse electric field $\vec{E} = E_y\hat{y}$ along the *y*-direction. Force due to this electric field, $q\vec{E}$opposed the Lorentz force $\vec{F}_B$and prevents further charge accumulation. In the steady state condition, these two forces balance out each other and we get,

$$qE_y = qvB \tag{3}$$

Now we define a quantity called *Hall coefficient* R_H, as the ratio of the electric field *Ey* to the current density *Jx* multiplied by magnetic field *B*, that is

$$R_H = \frac{E_y}{J_x B} = \frac{1}{nq} \tag{4}$$

where we have used Eq. (3) and the fact that $Jx = nqv$, *n* being the number density (m^{-3}) of charge carriers. In order to determine R_H, we proceed as follows. Writing $v = Jx/nq$ and multiplying both sides of Eq. (3) by *wd*, we get

$$E_y wd = \frac{J_x wdB}{nq} \tag{5}$$

But $Ew = V_H$, the voltage across the top and bottom surfaces called the Hall voltage and $J_x wd = I_H$. This gives,

$$V_H = \left(\frac{R_H B}{d}\right) I_H \tag{6}$$

Therefore, if we measure the Hall voltage V_H against Hall current I_H for a fixed magnetic field B and plot V_H versus I_H, the curve will be a straight line with the slope m being,

$$m = \frac{R_H B}{d} \tag{7}$$

The Hall coefficient R_H can be calculated from the value of this slope, m if the thickness d of the sample is known. Once R_H is determined, the carrier density n can be calculated using Eq. (4).Now assume the situation where the charge carriers are negative with $q = -e$. In that case, for current direction along $+x$, the charges will be moving with velocity $\vec{v} = -v\hat{x}$. The Lorentz force, $\vec{F}_B = q(\vec{v} \times \vec{B}) = -(evB)\hat{y}$ will still be along negative y direction as before. However this time, the bottom surface acquires negative polarity and consequently, the sign of the Hall voltage V_H will be opposite to what was observed in case of positive charge. Thus for given directions of the Hall current and the magnetic field, we can determine the type of charge carriers (whether +ve or -ve) by looking at the sign of the Hall voltage V_H.

Description of apparatus

The experimental setup is complete unit (Fig. 9.2) consisting of the followings - an electromagnet, constant current power supply, a Gauss and Tesla meter, a Hall current & voltage measurement unit and the sample connected with contact leads for passing Hall current and measuring Hall voltage.

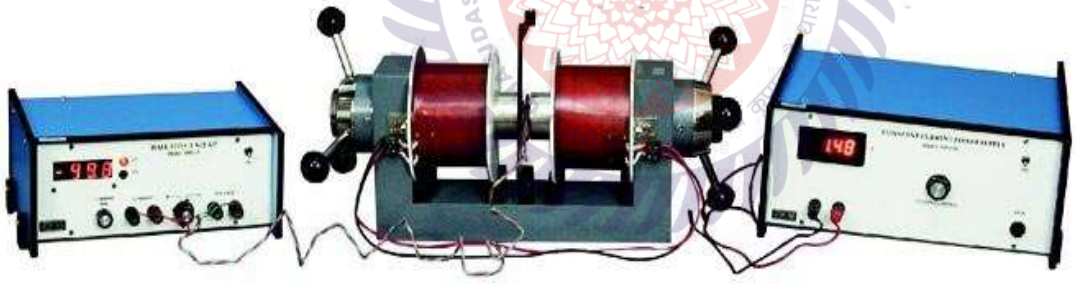


Fig. 9.2. Hall effect set-up

Experimental procedure:

1. Connect the width wise contacts of the Hall probe to the terminals marked ‘voltage’ and Length wise contacts to terminals marked ‘current’.
2. Switch ‘ON’ the Hall effect setup and adjustment current (say few mA).
3. Switch over the display to voltage side. There may be some voltage reading even outside the magnetic field. This is due to imperfect alignment of the four contacts of the Hall probe and is generally known as the ‘Zero field potential’. In case its value is comparable to the Hall voltage it should be adjusted to a minimum possible (for Hall probe (Ge) only). In all cases the error should be substracted from the Hall voltage reading.
4. Switch on the constant current power supply at any desired value.

5. Measure the magnetic field between the pole pieces of the electromagnet using digital Gaussmeter and also measure the distance between two pole pieces.
6. The Hall probe is placed in between the pole pieces of the electromagnet as shown in Fig. 9.2 and rotate the Hall probe till it becomes perpendicular to the magnetic field so that the Hall voltage will be minimum in this adjustment.
7. Measure the Hall voltage as a function of current in the Hall effect setup keeping the magnetic field constant and plot a graph.
8. The slopes (V_1 / I_1) &(V_2 / I_2) is to be calculated from the graph.

Determination of Hall Coefficient

The thickness of the semiconductor d = 0.58mm
Constant Power Supply: 1.5 A and 2 A

Data Sheet:

Sl. No.	**Const. Magnetic Field B_1 =…….Gauss**		**Const. Magnetic Field B_2 =…….Gauss**	
	Current in mA (I_1)	**Voltage in mV (V_1)**	**Current in mA (I_2)**	**Voltage in mV (V_2)**
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

Graph: A graph is plotted between Hall current (I) and Hall voltage (V) for two constant magnetic fields.

Calculation :

The value of Hall coefficient is calculated applying the formula $R_H = \frac{V_H d}{IB}$

From graph $\frac{V_1}{I_1}$=…… and $\frac{V_2}{I_2}$ =……

$$R_{H_1} = \frac{V_1 d}{I_1 B_1} =$$

$$R_{H_2} = \frac{V_2 d}{I_2 B_2} =$$

$$R_{H=} \frac{R_{H_1} + R_{H_2}}{2} =$$

Conclusion

Precautions

1. The current through the sample should not be large enough to cause heating.
2. The pressure contacts should be clean and firm to avoid noise.

WORK SHEET

AIM OF THE EXPERIMENT:

REQUISITES:

WORKING FORMULA :

The thickness of the semiconductor d = 0.58mm

Constant Power Supply: 1.5 A and 2A

Data Sheet:

Sl. No.	Const. Magnetic Field B_1 =……Gauss		Const. Magnetic Field B_2 =……Gauss	
	Current in mA (I_1)	Voltage in mV (V_1)	Current in mA (I_2)	Voltage in mV (V_2)
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

CALCULATION:

$R_{H_1} =$

$R_{H_2} =$

Mean $R_H =$

CONCLUSION

GRAPH SHEET

DETERMINATION OF HALL COEFFICIENT BY USING HALL APPARATUS

Voltage (V_H) VsCurrent (I)

Scale:

1. P-N JUNCTION DIODE CHARACTERISTICS

Experiment 1. Draw the VI Characteristics of given PN Junction diode. Determine the Static and Dynamic resistance of the Diode.

AIM:

1. To observe and draw the Forward and Reverse bias V-I Characteristics of a P-N Junction diode.
2. To calculate static and dynamic resistance in both forward and Reverse Bias Condition.

APPARATUS:

1. P-N Diode IN4007 - 1No.
2. Regulated Power supply (0-30V) - 1No.
3. Resistor 1KΩ, 10KΩ - 1No.
4. Ammeter (0-20 mA) - 1No
5. Ammeter (0-200μA) - 1No.
6. Voltmeter (0-20V) - 2No.
7. Bread board
8. Connecting wires

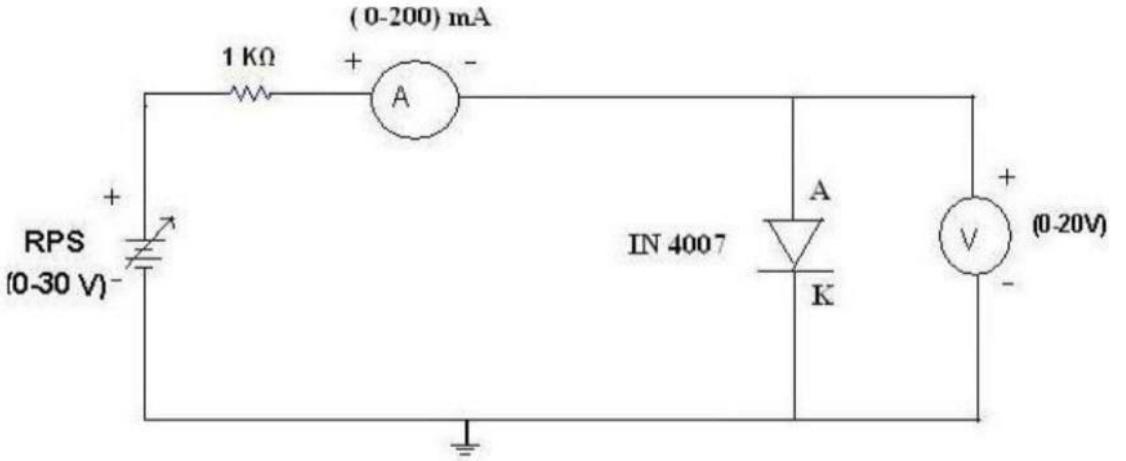
THEORY:

A P-N junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current flowing through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode) is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. Then diode is said to be in ON state. The current increases with increasing forward voltage.

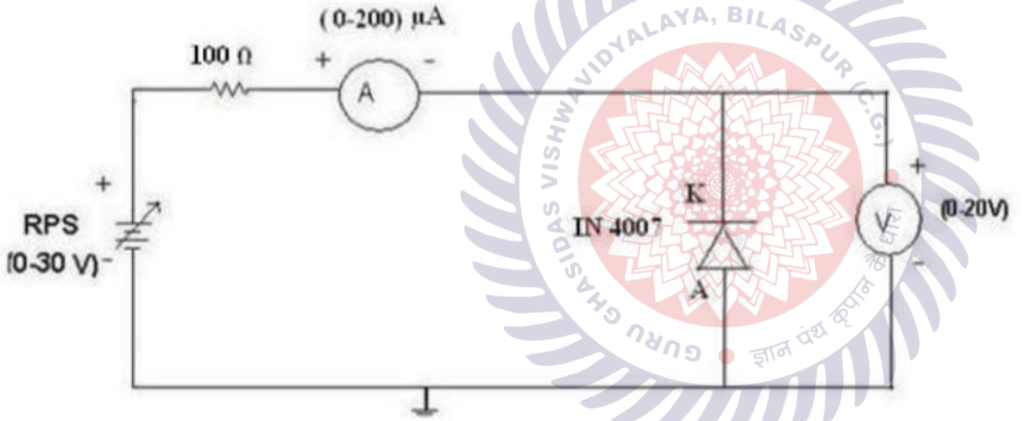
When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. Then diode is said to be in OFF state. The reverse bias current is due to minority charge carriers.

CIRCUIT DIAGRAM:

A) Forward bias:



B) Reverse Bias:



PROCEDURE:

A) FORWARD BIAS:

1. Connections are made as per the circuit diagram.
2. for forward bias, the RPS +ve is connected to the anode of the diode and RPS –ve is connected to the cathode of the diode
3. Switch on the power supply and increases the input voltage (supply voltage) in Steps of 0.1V
4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.
5. The reading of voltage and current are tabulated.
6. Graph is plotted between voltage (V_f) on X-axis and current (I_f) on Y-axis.

B) REVERSE BIAS:

1. Connections are made as per the circuit diagram

2. For reverse bias, the RPS + ve is connected to the cathode of the diode and RPS –ve is connected to the anode of the diode.
3. Switch on the power supply and increase the input voltage (supply voltage) in Steps of 1V.
4. Note down the corresponding current flowing through the diode voltage across the diode for each and every step of the input voltage.
5. The readings of voltage and current are tabulated
6. Graph is plotted between voltage (V_R) on X-axis and current (I_R) on Y-axis.

OBSERVATIONS:

A) FORWARD BIAS:

S. No	Applied Voltage (V)	Forward Voltage (Vf)	Forward Current If (mA)

B) REVERSE BIAS:

S. No	Applied Voltage (V)	Reverse Voltage (Vr)	Forward Current Ir (uA)

Calculations:

Calculation of Static and Dynamic Resistance for a given diode

In forward bias condition:

Static Resistance, $R_s = V_f / I_f =$

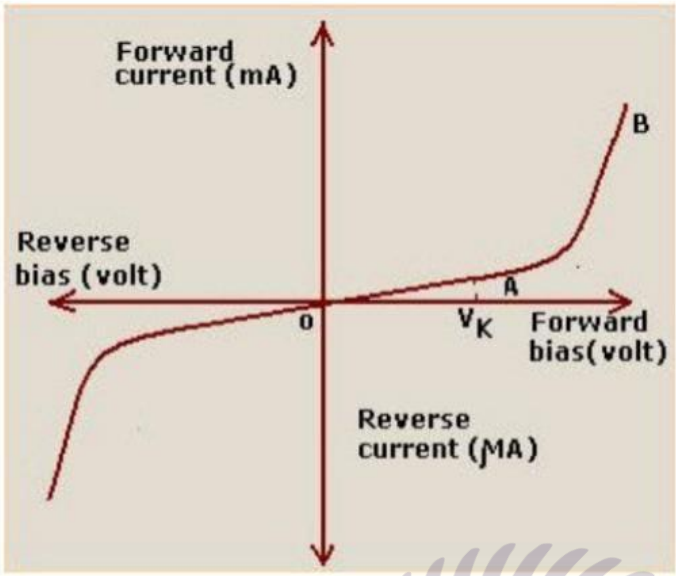
Dynamic Resistance, $R_D = \Delta V_f / \Delta I_f =$

In Reverse bias condition:

Static Resistance, $R_s = V_R / I_R =$

Dynamic Resistance, $R_D = \Delta V_R / \Delta I_R =$

MODEL GRAPH:



PRECAUTIONS:

1. All the connections should be correct.
2. Parallax error should be avoided while taking the readings from the Analog meters.

RESULT:

1. Cut in Voltage = _____V
2. Static forward resistance = _____
3. Dynamic forward resistance = _____

VIVA QUESTIONS:

1. Define depletion region of a diode?
2. What is meant by transition & space charge capacitance of a diode?
3. Is the V-I relationship of a diode Linear or Exponential?
4. Define cut-in voltage of a diode and specify the values for Si and Ge diodes?
5. What are the applications of a p-n diode?
6. Draw the ideal characteristics of P-N junction diode?
7. What is the diode equation?
8. What is PIV?
9. What is the break down voltage?
10. What is the effect of temperature on PN junction diodes?
11. Specifications of diodes

TO STUDY THE CHARACTERISTICS OF SOLAR CELL

OBJECT

To study the characteristics of solar cell, the following studies can be carried out.

1. Illumination Characteristics.
2. Current Voltage Characteristics.
3. Power Load Characteristics.
4. Area Characteristics.
5. Spectral Characteristics.

OPTIONAL

1. Distance Vs Open Circuit Voltage.
2. Distance Vs Short Circuit Current.
3. Measurement of Short Circuit Current (I_{ESC}) with biasing the solar cell and compare it with the theoretical value obtained from current voltage characteristics curves.

THEORY:

Solar cells are basically solid-state devices. It is basically a p-n junction, which converts sunlight (solar energy) into electrical energy through a three-step process:

1. **Generation of carrier pairs (electron hole pairs)**
2. **Separation of electrons and holes**
3. **Collection of separated carriers**

The details of each of the three processes are beyond the scope of this manual. Pl see text books.

When a solar cell is illuminated, the photons incidents on the cell generate electrons-hole pairs. By diffusion in the material the electron and holes reach the junction. At the junction the barrier field separates the positive and negative charges carriers. Under the action of the electric field, the electrons (minority carriers) from p region are swept into n region. Similarly, the holes from n region are swept into p region. It leads to an increase in the number of holes on the p side and of the electrons on the n side of the junction. The accumulation of charges on the two sides of the junction produces an emf, which is called a photo emf. The photo emf is known as open circuit voltage. It is proportional to the illumination (mW/cm^2 or $lumen/cm^2$) and on the size of the illuminated area. When an external circuit is connected across the solar cell terminals, the minority carriers return to their original sides through the external circuit, causing the current to flow through the circuit. Thus the solar cell behaves as a battery with n side as the negative terminal and p side as positive terminal. The photo emf or voltage can be measured with a voltmeter. The process of generation of photovoltaic voltage is shown in Fig.

(1) The conversion of optical energy is known as photovoltaic effect. Hence a solar cell is also called a photovoltaic cell.

All solar cell materials used till date are semiconductors in crystalline or amorphous forms. A common characteristic of these materials is that they posses a band gap i.e. a discontinuity or rather a range of forbidden values in the energy spectrum. Mostly, solar cells are fabricated from silicon single crystals; Silicon is not transparent for visible light. Therefore, the surface layer of the cell, which is of p type, is made extremely thin to enable maximum light to penetrate the junction. It is desired the absorption of light takes place at the junction region such that the generated electron holes pairs can be separated by the junction fields before they are lost by recombination. To enhance the transmission of the light into the material an anti reflection coating is given over p type layer. Thin metallic films vacuum deposited suitably on both the sides of the cell act as electrodes. An open

circuit voltage of peak value of 0.6 V is generated by a solar cell. Silicon wafer of 1"dia to 4"dia are used too fabricate solar cells. In order to enhance the total voltage and current out put, a number of P-n junction are formed on a wafer, using a mesh type or finger like electrode structure. To increase power output, solar cells are arrayed into a series chain or parallel chain and are interconnected. Such an arrangement is called a solar panel. In normal use single solar cell is rarely used, as its output is very low.

(i) **Illumination Characteristic**

The Illumination Characteristic of a solar cell is shown in the Fig. (2). It is seen that the current through the solar cell increases as the intensity of the light falling on the solar cell increases.

(ii) **Current Voltage Characteristic**

The out put characteristic (current voltage characteristics) of a solar cell is shown in the Fig. (3) it is seen that in the open circuit, the out put voltage of the cell is ≈ 0.6 V and the current is zero. If the panel is short circuited, the current is maximum while the output voltage of the cell becomes zero. In both the cases, the output power is zero. It is seen from the curve that the voltage varies depending on the current drawn.

(iii) **Power Load Characteristics**

To derive maximum power from the panel, an appropriate load is to be connected across it. The value of the load that allows the cell to give maximum output power is obtained by drawing a power load characteristics, as shown in the Fig. (4). It is seen that a load other than $(R_L)_{max}$ will produce less power.

(iv) **Area Characteristics:**

The power delivered is proportional to the surface area of the solar panel exposed to the light. It is governed by the relation,

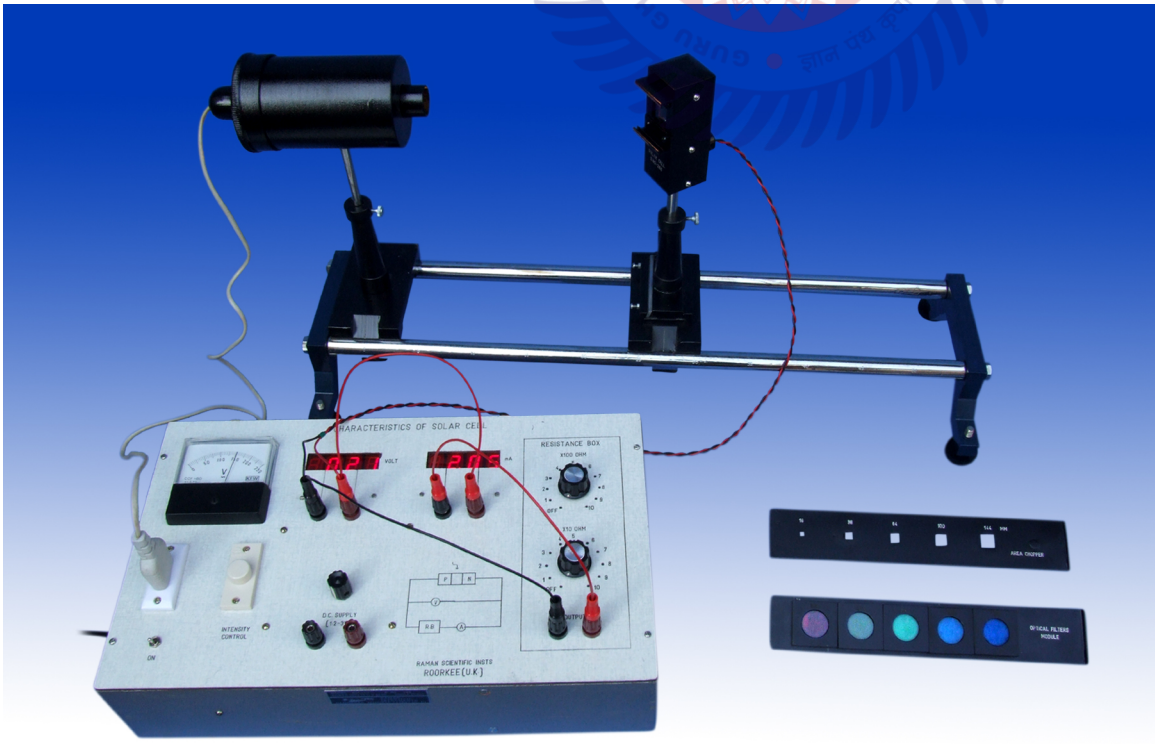
$$P = K A$$

Where, P is the total power available
A is the area of the Cell
K is a constant.

The dependence of P on A is shown in the Fig. (5)

(v) **Spectral Characteristics:**

The response of a solar cell to light depends on the wavelength of the incident light also. In the sunlight, different colors have different intensities. The variation of power on wavelength is shown in the Fig.(6)



PROCEDURE

(a) Illumination Characteristics

1. Make the circuit as shown in fig. 7. A 100 W lamp is arranged over the solar cell such that the light falls on it at normal. The intensity control is kept at its minimum say at 50 volts and the lamp is switched on.
2. Adjust the resistance box at zero ohm (i.e. both the knobs marked X10 and X100 ohm must be set at off position) note the short circuit current and make table as shown below.
3. Increase the intensity of the lamp in steps say 100, 150, 200 volts and note the corresponding current for each setting of the voltage, record these readings in the table.

Note: Intensity is taken as proportional to the A.C. voltage given to the lamp

a. Plot a graph between Current and the Intensity.

Table – 1

S.No.	Intensity (volts)	Current (mA)
1. 2. 3.		

(b) Current Voltage Characteristics

1. The intensity of the lamp is kept at the minimum say 100 V. disconnect the load resistance (i.e. R.B. is at infinity) and note the open circuit voltage.
2. Adjust the resistance box (R.B.) at zero ohm (i.e. both the knob of the resistance box marked X10 and X100 ohm must be set at off position) and note the short circuit current.
3. Set the load dial at 100 ohms. Note the corresponding voltage and current make the table as shown below and record these readings in the table. Vary the load in steps up to 1100 ohms and note the corresponding voltage and current for each setting of the load in table
4. The intensity of the lamp is increased say 150 V. The load is again varied from 100 to 1100 ohms and note the corresponding voltage and the currents, record the value in the table. The open circuit voltage and the short circuit current are also determined and recorded.
5. The intensity of the lamp is set at 200 V, and repeat step 4. Record these readings in the table.
6. Plot a graph for Current Vs Voltage.

Table – 2

S.No.	R_L Ohms	Intensity, I_1		Intensity, I_2		Intensity, I_3	
		Voltage(V)	Current(mA)	Voltage(V)	Current(mA)	Voltage(V)	Current(mA)
1. 2. 3.	100 200 ….						

(c) Power Load Characteristics

1. Using the sets of the reading obtained in the table 2 above, calculate the output power of the cell. Make table as shown below and record the readings in the table.
2. Plot a graph for Power Vs Load. Measure the value of the optimum load that draws maximum power from the cell.

Table – 3

S.No.	R_L Ohms	Intensity, I_1 = 100 V	Intensity, I_2 = 150 V	Intensity, I_3 = 200 V
		Power mW	Power mW	Power mW
1. 2. 3.	100 200 ….			

(d) Area Characteristics:

1. Set the intensity of the lamp at a convenient level say 200V. Adjust the load at the optimum value.
2. Place the chopper plate having different slot areas, in front of the solar cell in the grove provided.
3. Adjust one of the slot say 16 mm^2 over the solar cell; it reduces the surface area, which is illuminated. The voltage and the current readings are noted in the table. Note the corresponding voltage and current readings make table as shown below and record the readings in the table.
4. Adjust the other slots say 36, 64, 100, 144 mm^2 over the solar cell and note the corresponding current and voltage for each slot area and record the readings in the table.
5. Plot a graph for Power Vs Area. Measure the slope of the curve.

Table – 4

S.No.	Slot Area mm^2	Voltage, V volts	Current, I amp	Power P = VI mW
1. 2. 3. 4.				

(e) Spectral Characteristics:

1. Set the intensity of the lamp to a convenient level say 200 V. Adjust the load at the optimum value.
2. Put the different colors filter over the solar cell and for each filter the note voltage and the current and record these readings in the table.
3. The wavelength corresponding to each color is noted and calculate the output power
4. Plot a graph for Power Vs Wavelength.

Table – 5

S.No.	Filter Colors	Peak Wavelength Transmitted, A^o	Voltage, V volts	Current, I amp	Power P = VI mW
1. 2.					

OPTION-

Distance Vs Open Circuit Voltage:
Repeat step 1 of the current voltage characteristics and vary the distance between the source and the photocell and not the open circuit voltage for each position of the cell from the source say at 15, 18, 21, 24, 27, 30 cm.

Distance Vs Short Circuit Current:
Repeat step 2 of the current voltage characteristics and vary the distance between the source and the photocell and note the short circuit current for each position of the cell from the source say at 15, 18, 21, 24, 27, 30 cm.

Experimental Measurement of Short Circuit Current:
Make the circuit as shown in the fig. 7(b) using R_2 and the multimeter. Set the lamp voltage say at 100 volts. Adjust the supply voltage at 1.5 volts and vary R_2 till the voltmeter V reads Zero voltage. In this position the cell and the battery try to send current through R.B. and when both currents are equal no current will pass through R.B. and thus no voltage drop across it as measured by the voltmeter. In this case, the current obtained through multimeter gives the short circuit current. Repeat the experiment for different values of lamp voltage say150, 200 volts and note the corresponding short circuit current. Make table as shown below:

Table - 6
Compare the Experimental value of Short Circuit Current I_{ESC} with the Theoretical value.

S.No.	Lamp Voltage	Experimental value of Short circuit current I_{ESC}	Theoretical value of Short circuit current obtained from V-I characteristics curve.
1. 2. 3.			

P)

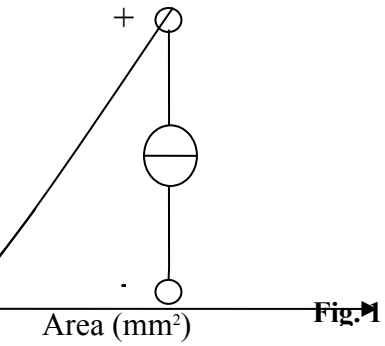


Fig. 1

Fig. 5

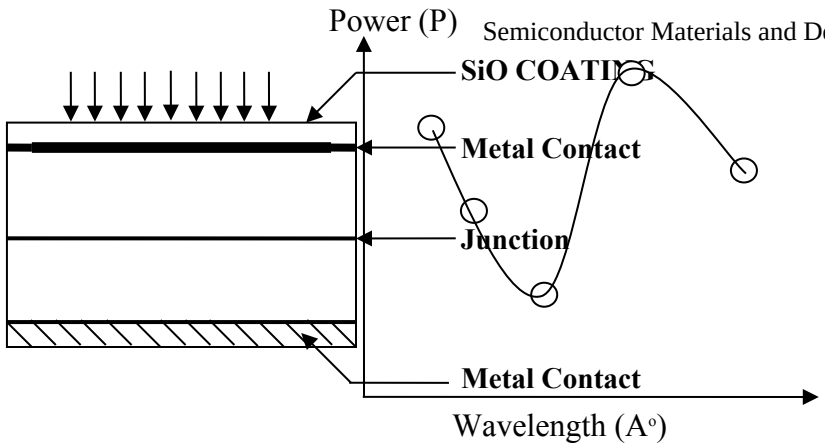


Fig. 6

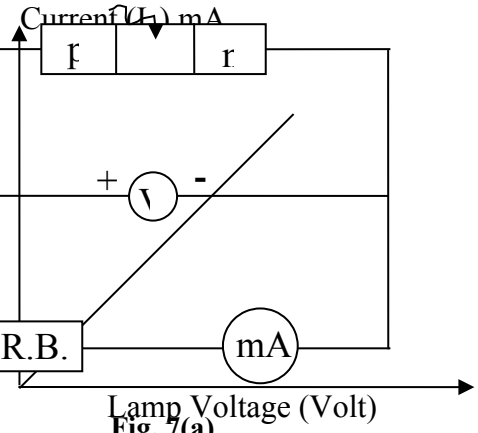


Fig. 7(a)

Fig. 2

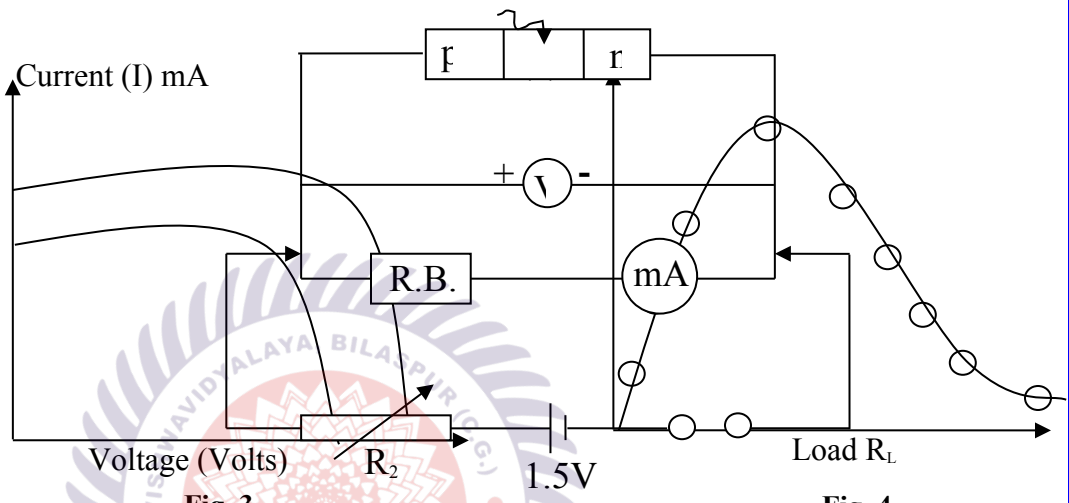


Fig. 3

Fig. 7(b)

Fig. 4

GURU GHASIDAS VISHWAVIDYALAYA, BILASPUR (C.G.)
ज्ञान पंथ कृपान के धारा

1. Characteristics of Junction Field Effect Transistor (JFET)

Aim:

To study the Drain and Transfer Characteristics of a Junction Field Effect Transistor (JFET).

Components:

JFET (BFW10), Bread board, Regulated Power supply (0 - 2 V) and (0 - 12 V), Ammeters (0 - 20 mA), Voltmeter V_1 (0 - 2V), Voltmeter V_2, (0 - 10V), Connecting wires (Single Strand)

Theory and Operation:

1. Drain characteristics are obtained between the drain to source voltage ($\mathbf{V_{DS}}$) and drain current ($\mathbf{I_D}$) taking gate to source voltage ($\mathbf{V_{GS}}$) as the constant parameter.
2. Transfer characteristics are obtained between the gate to source voltage ($\mathbf{V_{GS}}$) and drain current ($\mathbf{I_D}$) taking drain to source voltage ($\mathbf{V_{DS}}$) as the constant parameter.

FET Parameters

1. **Drain Resistance (r_d):** It is given by the relation of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in Drain Current (ΔI_D) for a constant gate to source voltage (ΔV_{GS}), when the JFET is operating in pinch-off region.

   $r_d = \frac{\Delta V_{DS}}{\Delta I_D}$ at a constant $\mathbf{V_{GS}}$ (from drain characteristics)

2. **Trans Conductance (g_m):** Ratio of small change in drain current (ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant $\mathbf{V_{DS}}$.

   $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ at constant $\mathbf{V_{DS}}$ (from transfer characteristics).

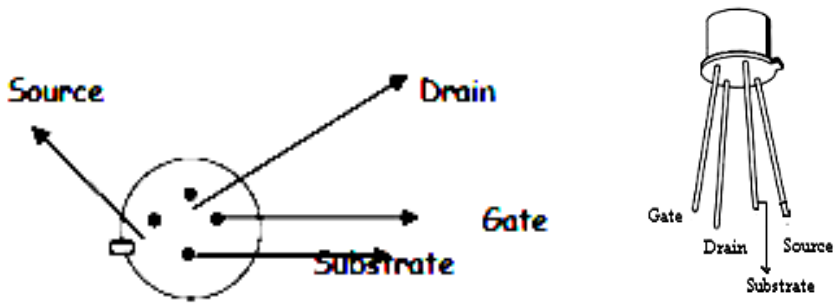
   The value of g_m is expressed in mho's ($\mho$) or Siemens (**s**).

3. **Amplification factor (μ):** It is given by the ratio of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant drain current (I_D).

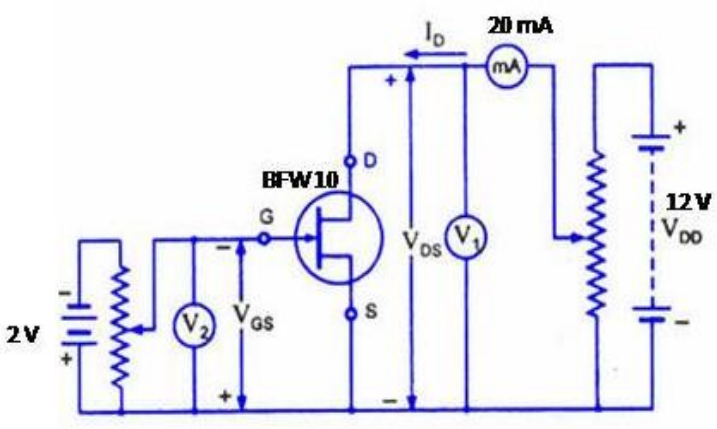
   $\boldsymbol{\mu = \left(\frac{\Delta V_{DS}}{\Delta I_D}\right) \times \left(\frac{\Delta I_D}{\Delta V_{GS}}\right) = \frac{\Delta V_{DS}}{\Delta V_{GS}}}$

   ie. $\boldsymbol{\mu = r_d \times g_m}$

Pin assignment of FET:



Circuit Diagram:



Procedure:

Drain Characteristics:

1. Connect the circuit as shown in the figure1.
2. Keep **V_{GS} = 0V** by varying **V_{GG}**.
3. Varying **V_{DD}** gradually in steps of **1V** up to **10V** note down drain current **I_D** and drain to source voltage (**V_{DS}**).
4. Repeat above procedure for **V_{GS} = -0.4, -0.8, -1.2** and **-1.6 V**

Transfer Characteristics:

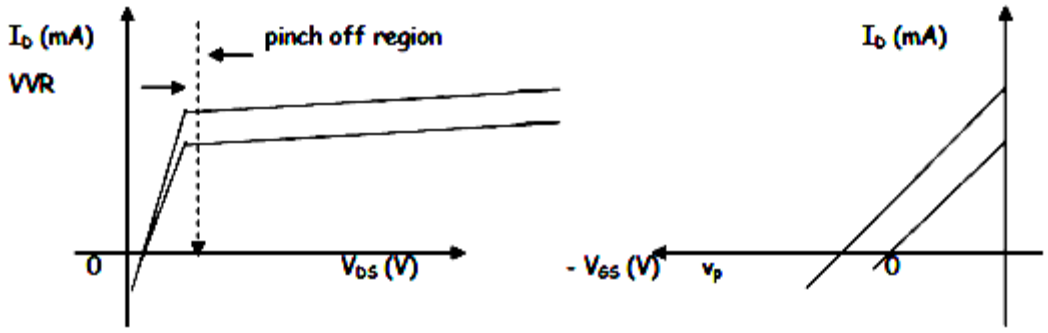
1. Connect the circuit as shown in the figure1.
2. Set voltage **V_{DS} = 4V/8V**
3. Varying **V_{DS}** in steps of 0.5V until the current **I_D** reduces to minimum value.
4. Varying **V_{GG}** gradually, note down both drain current **I_D** and gate-source voltage (**V_{GS}**).
5. Repeat above procedure (step 3) for **V_{DS}** = 4V/ 8V

Observations:

Drain Characteristics						
V_{DS} (Volts)	**V_{GS} = 0V**		**V_{GS} = -0.4V**		**V_{GS} = -0.8V**	**V_{GS} = -1.2V**
	V_{DS}(Volts)	**I_D(mA)**	**V_{DS}(Volts)**	**I_D(mA)**	**V_{DS}(Volts)**	**I_D(mA)**
0						
2						
4						
6						
8						
10						

Transfer Characteristics			
V_{DS} = 4V		**V_{DS} = 8V**	
V_{GS}(Volts)	**I_D(mA)**	**V_{GS}(Volts)**	**I_D(mA)**
0			
0.5			
1.0			
1.5			

Graph:



DRAIN CHARACTERISTICS **TRANSFER CHARACTERISTICS**

1. Plot the drain characteristics by taking $\mathbf{V_{DS}}$ on X-axis and $\mathbf{I_D}$ on Y-axis at a constant $\mathbf{V_{GS}}$.
2. Plot the transfer characteristics by taking $\mathbf{V_{GS}}$ on X-axis and taking $\mathbf{I_D}$ on Y-axis at constant $\mathbf{V_{DS}}$.

Calculations from Graph:

1. **Drain Resistance (r_d):**
   $r_d = \frac{\Delta V_{DS}}{\Delta I_D}$ at a constant $\mathbf{V_{GS}}$ (from drain characteristics)
2. **Trans Conductance (g_m):**
   $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ at constant $\mathbf{V_{DS}}$ (from transfer characteristics).

   The value of $\mathbf{g_m}$ is expressed in mho's (℧) or Siemens (**s**).

3. **Amplification factor (μ):** It is given by the ratio of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant drain current (I_D).
   $\boldsymbol{\mu = \left(\frac{\Delta V_{DS}}{\Delta I_D}\right) \times \left(\frac{\Delta I_D}{\Delta V_{GS}}\right) = \frac{\Delta V_{DS}}{\Delta V_{GS}}}$
   ie. $\boldsymbol{\mu = r_d \times g_m}$

Result: Drain and Transfer characteristics of a FET are studied.

Outcomes: Students are able to

1. Analyze the Drain and transfer characteristics of FET in Common Source configuration.
2. Calculate the parameters transconductance (g_m), drain resistance ($\mathbf{r_d}$) and amplification factor (**μ**).

THEORY

Transistor is a 3-terminal and 2-junction (p-n) device. Its name comes from transfer + resistance. The current through 2 terminals can be controlled by I/V through the other 2 terminals.

Broad classification –

a) BJT (Bipolar Junction Transistor) – Current-controlled device

b) FET (Field Effect Transistor) – Voltage-controlled device

i) JFET (Junction FET) – n-channel is already formed

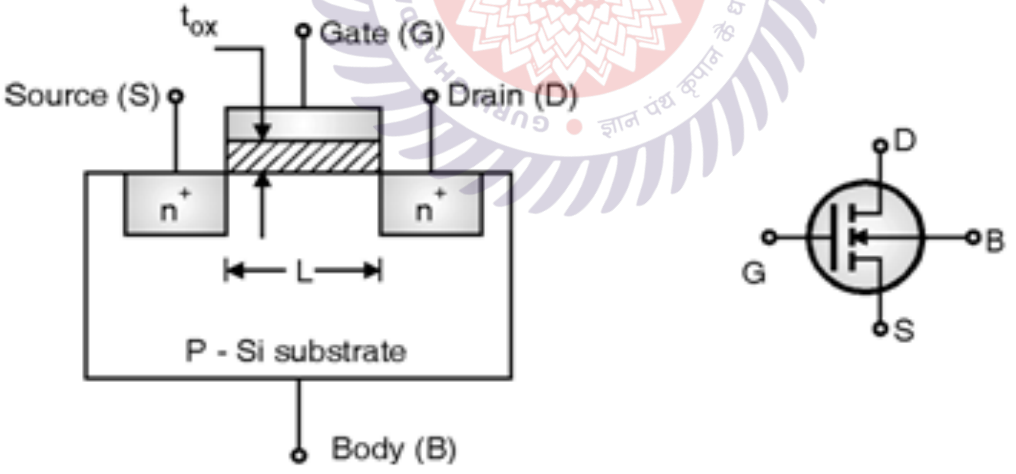
ii) E-MOSFET (Metal Oxide Semiconductor FET) – n-channel has to be formed

A FET has three terminals as:

1) Source (S): The terminal through which the majority charge carriers enter the channel. Conventionally, current entering at S is designated by I_S.

2) Drain (D): The terminal through which the majority charge carriers leave the channel. Conventionally, current entering the channel at D is designated by I_D. Drain-to-source voltage is V_{DS}.

3) Gate (G): the terminal that modulates the channel conductivity.



(a) Cross sectional view **(b) Symbol**

n-channel enhancement mode MOSFET

t_{ox} is the thickness of the oxide layer (generally SiO_2), L is the channel length

Figure 1. Basic structure of MOSFET

MOSFET is a field effect transistor whose drain current (I_D) is controlled by the voltage on the gate (see Figure 1). MOSFET has a much higher input impedance because of the very small gate leakage current. It has wide applications in the field of modern-era digital circuits. It is used in the amplification of the signal and switching action. Its major advantage over BJT in switching is that it is much more power efficient at high-frequency switching. It has a +ve temperature coefficient, so it is thermally stable.

MOSFET is of 2 types: a) enhancement type - n & p type

b) depletion type - n & p type

The experiment will be done with n-enhancement type MOSFET.

Depletion/Space Charge Region –

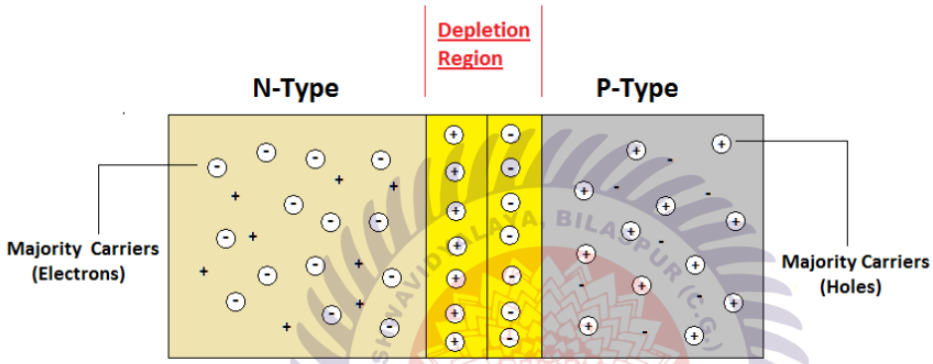


Figure 2. Depletion region in a p-n junction

There is a greater concentration of holes in the P-region and electrons in the N-region. This difference in concentration establishes a mismatch across the junction resulting in majority carrier diffusion. Holes diffuse from P to N and electrons from N to P regions causing the recombination. This recombination of electrons and holes produces a narrow region at the junction called the depletion region as shown in Figure 2.

N-channel formation and Pinch-off phenomena

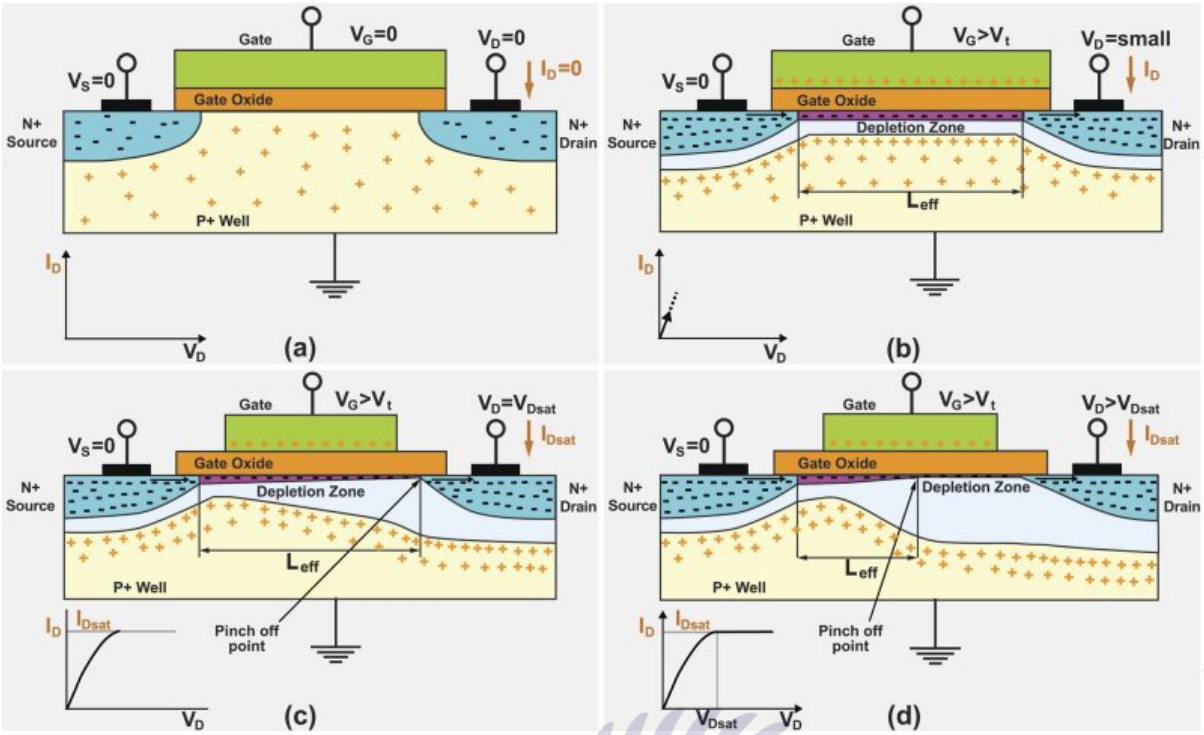


Figure 3 (a) $V_G = 0$, no biasing between Gate & Source, 3 (b) $V_G > V_T$, forward bias to Gate w.r.t to Source. The -ve charge is pulled towards Gate. Thus, at a particular point number of electrons > number of holes within the depletion region. So, there is a creation of a region where n-type conductivity opposed to p-type is formed. This is called the inversion region. Hence n-channel is formed through which electrons can flow. 3 (c) $V_D = V_{DSat} = V_{GS} - V_T$, transition from ohmic region to saturation region, 3 (d) $V_D > V_{DSat}$, pinch-off point moves towards the Source thus reducing the channel length. Under these conditions, the area between the pinch-off point and the drain is fully depleted with no inversion layer. Since this region has no positive free carriers, there is no possibility for electron-hole recombination if an electron enters the region from the electron-rich source and, if there is an electric field across the depletion zone, the electron can freely transit to the drain. The current through the device becomes controlled solely by the gate voltage under drain saturation conditions.

MOSFET CHARACTERISTICS APPARATUS

Instrument Specifications –

1) Two continuously variable DC-regulated power supplies of 0-5 V for gate and 0-30 V for Drain & Gate voltage are provided.

Input Voltage	: 230V±10% AC , 50Hz
Load Regulation	: ±0.2%
Line Regulation	: ±0.05%
Ripple	: Less than 3mV R.M.S

Protections : Against Short Circuit & Overload

2) Three meters to measure voltage & current are mounted on the front panel & connections are brought out on at Sockets.
3) One N-channel enhancement type MOSFET No. IRF 840 is placed behind the cabinet & connections are brought on at sockets

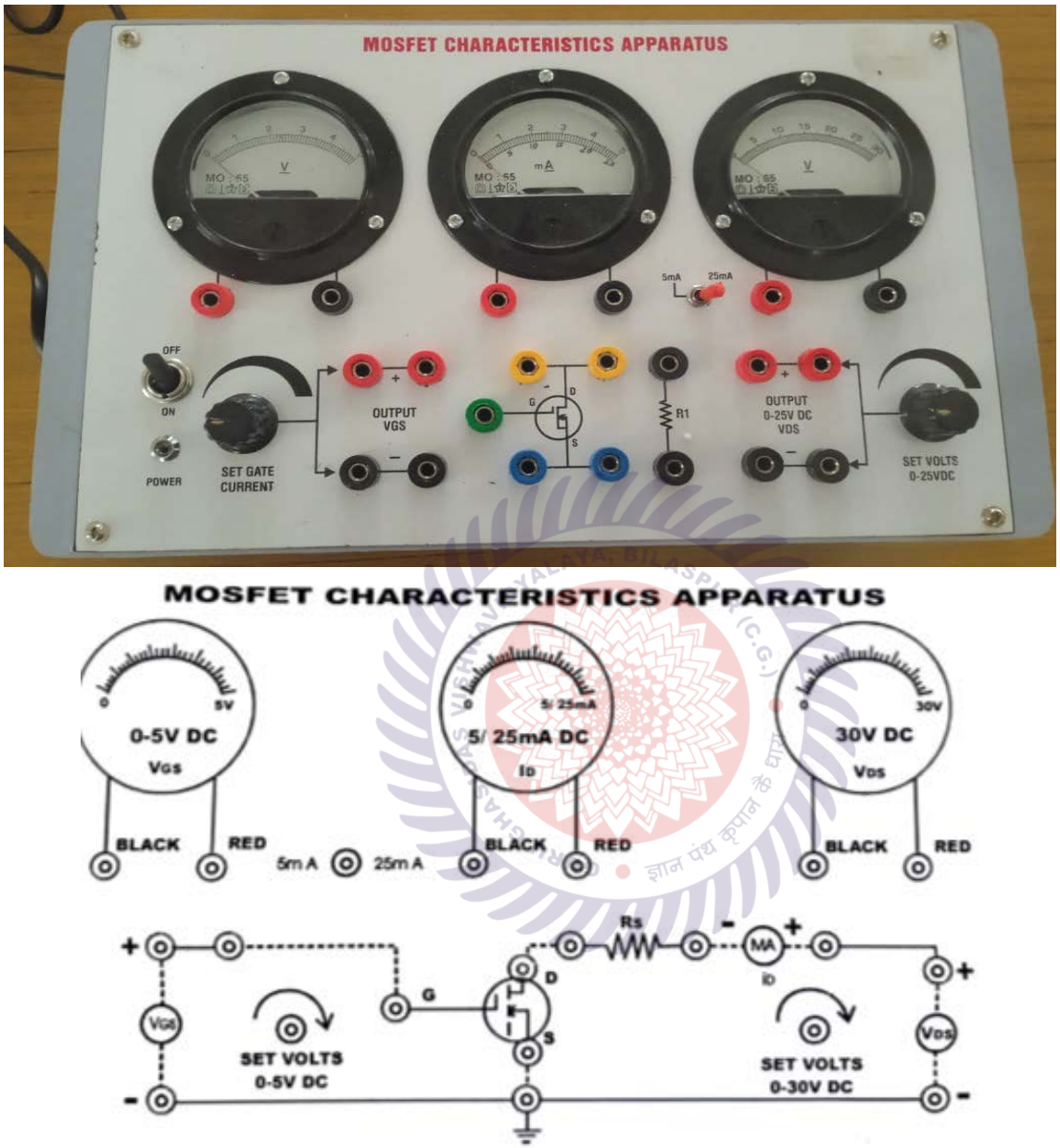


Figure 4. MOSFET Characteristics Apparatus and circuit diagram

Precautions –

1) Make sure all the voltage and current are set to 0 before applying the DC supply.
2) Increase the voltage slowly and note the reading very carefully to avoid parallax error.

Experiment 1 – To study the transfer characteristics of MOSFET and find out the threshold voltage

Objective – To find out the threshold voltage and transconductance of the MOSFET device.

Threshold Voltage (V_{TH}) - Threshold voltage, for an enhancement-type MOSFET, is the minimum amount of gate-to-source voltage which must be applied to create an inversion region for the conduction of charge carriers across the device, between the drain and the source, on the application of suitable bias between them (see Figure 4).

Transconductance (gm) – It is the ratio of the current change at the output port to the voltage change at the input port as depicted in Figure 4.

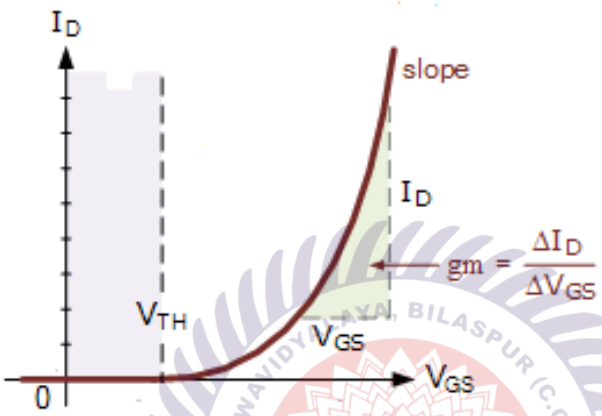


Figure 5. Threshold voltage (V_{TH}) and transconductance (gm) of the MOSFET device.

Procedure –

1) Connect the circuit as shown in Figure 4.
2) Keep control knobs of both the Power supplies anticlockwise & switch on the instrument by changing the position of the toggle switch to the ON side provided on the front panel. LED provided on the front panel will glow indicating that the instrument is ready for use.
3) Keep V_{DS} constant at 20 Volts.
4) Increase the V_{GS} in forward bias and note down I_D in Table 1.
5) Plot a graph between V_{GS} and I_D and **find V_{th}.**

Table 1. **Fill in the values just when $I_D \neq 0$**

Sl. No	$V_{DS} = 20V$	
	$V_{GS}(V)$	$I_D(mA)$
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		

Results –

1) Plot the transfer characteristics curve (I_{DS} vs V_{GS}).
2) Calculate the transconductance and write the threshold voltage.

Experiment 2 – To study the Drain characteristics of MOSFET

Objective – To know about ohmic, saturation & cut-off region in the drain characteristic plot. Also, to get an idea about the pinch-off point.

A) Ohmic/triode region –

$$I_D = k[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

for small values of V_{DS},

$$I_D = k[2(V_{GS} - V_T)V_{DS}]$$

$$I_D \propto V_{DS} \text{ (linear)}$$

B) Saturation region –

$$V_{DS} \geq (V_{GS} - V_T)$$
$$I_D \neq f(V_{DS}) \quad \text{(almost true)}$$

C) Cut-off region –

$$V_{GS} < V_T$$
$$I_D = 0 \text{ (Device is OFF)}$$

Procedure –

1) Connect the circuit as shown in Figure 4.
2) Keep control knobs of both the Power supplies anticlockwise & switch on the instrument by changing the position of the toggle switch to the ON side provided on the front panel. LED provided on the front panel will glow indicating that the instrument is ready for use.
3) Keep V_{GS} (Gate to Source Voltage) constant at $V_{Th} + 0.1$.
4) Keep Drain to Source voltage at 0.5 V & note down the corresponding Drain current.
5) Increase the drain-source voltage in small steps (0.5V) and note the effect of that voltage on the drain current I_D.
6) Now repeat steps 4&5 for different Gate voltages (V_{GS}) as mentioned in Table 2 and note down the observations.

Table 2

Sl. No	$V_{GS} = V_{Th} + 0.1$		$V_{GS} = V_{Th} + 0.3$		$V_{GS} = V_{Th} + 0.4$	
	V_{DS}	I_D	V_{DS}	I_D	V_{DS}	I_D
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						
17						
18						
19						
20						
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22						
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27						
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33						
34						
35						
36						
37						
38						
39						
40						
41						
42						
43						
44						
45						
46						

47						
48						
49						
50						

Results –

1) Plot the drain characteristics curve indicating –
   a) Pinch-off points
   b) Ohmic/triode region
   c) Saturation region

   For all V_{GS}

2) Calculate $R_{DS}(ON)$ for different V_{GS}.
   Plot R_{DS} vs V_{GS}. Does it increase or decrease on increasing V_{GS} and why?

<u>Analysis</u> –

1. Which region is used for amplification? Why?
2. How n-channel MOSFET is better than p-channel MOSFET in switching action?
3. What is the physical significance of transconductance?
4. How is n-channel getting formed in the MOSFET?
5. Explain the reason for saturation or pinch-off phenomena when V_{DS} increases.
6. Why I_D is varying with V_{DS} in the saturated region in the obtained plot? What should be the case for ideal MOSFET?