List of Experiment
B.Sc. IV Semester (Electronics) Core – 08
Operational Amplifier & Application Lab

1. Designing of an amplifier of given gain for an inverting and non-inverting configuration op-amp.

2. Designing of an analog adder and subtractor circuit.

3. Designing of an integrator using op-amp for a given specification & study of its frequency response.

4. Designing of a differentiator using op-amp for a given specification & study its frequency response.

5. Designing a first order Low-pass filter using op-amp.

6. Designing a first order High-pass filter using op-amp.

7. Designing of a RC Phase shift oscillator using op-amp.

8. Study of IC 555 as an astable multivibrator.

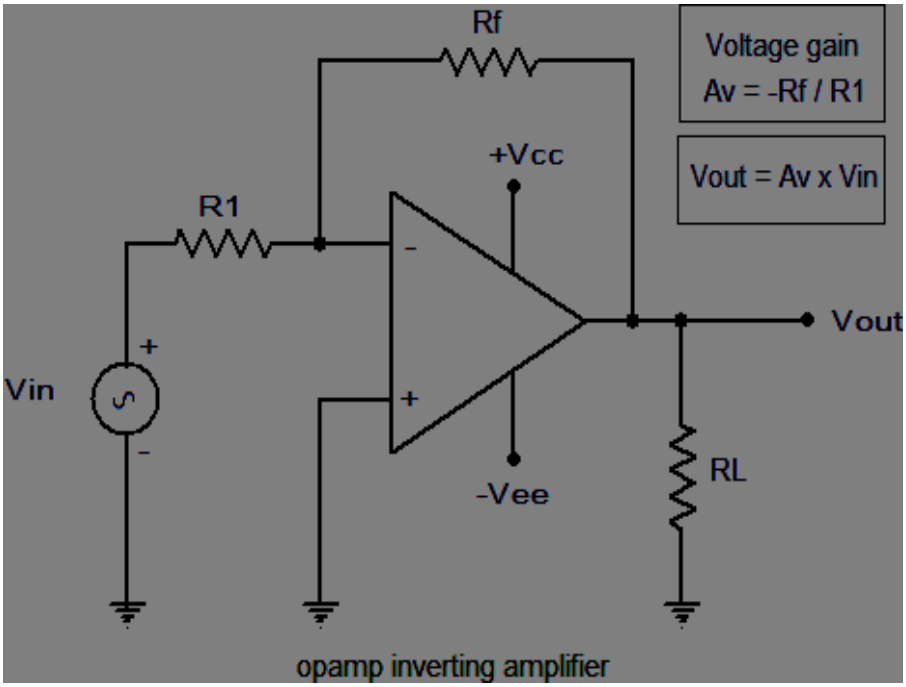
9. Study of IC 555 as an monostable multivibrator .

Experiment No 1

Objective: Designing of an amplifier of given gain for an Inverting and Non-inverting Configuration Op-amp.

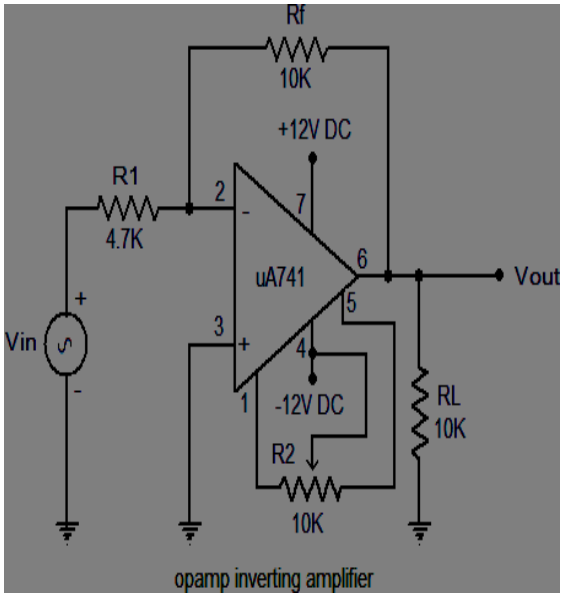
Apparatus Required: Bread Board, 741 IC, ±12V supply, Resistors and connecting leads.

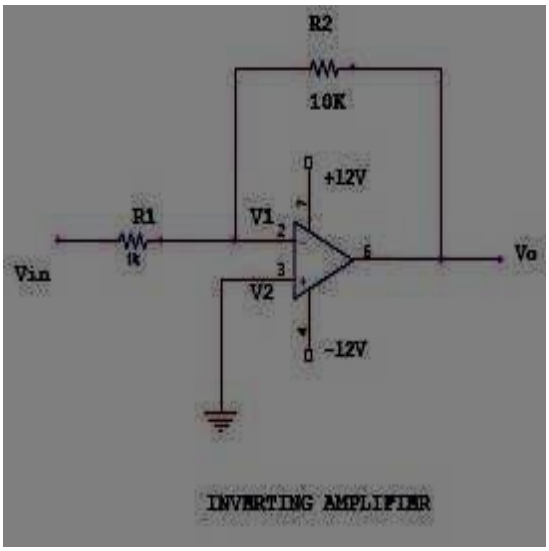
Theory: An inverting amplifier using op-amp is a type of amplifier using op-amp where the output waveform will be phase opposite to the input waveform. The input waveform will be amplifier by the factor Av (voltage gain of the amplifier) in magnitude and its phase will be inverted. In the inverting amplifier circuit the signal to be amplified is applied to the inverting input of the op- amp through the input resistance R1. Rf is the feedback resistor. Rf and Rin together determine the gain of the amplifier. Inverting operational amplifier gain can be expressed using the equation Av = – Rf/R1. Negative sign implies that the output signal is negated. The circuit diagram of a basic inverting amplifier using op-amp is shown below.



The input and output waveforms of an inverting amplifier using op-amp is shown below. The graph is drawn assuming that the gain (Av) of the amplifier is 2 and the input signal is a sine wave. It is clear from the graph that the output is twice in magnitude when compared to the input (Vout = Av x Vin) and phase opposite to the input. Practical inverting amplifier using 741. A simple practical inverting amplifier using 741 IC is shown below. uA 741 is a high performance and of course the most popular operational amplifier. It can be used in a verity of applications like integrator, Differentiator, voltage follower, amplifier etc. uA 741 has a wide supply voltage range (+/-22V DC) and has a high open loop gain. The IC has an integrated compensation network for improving stability and has short circuit protection. Signal to be amplified is applied to the inverting pi (pin2) of the IC. Non inverting pin (pin3) is connected to ground. R1 is the input resistor and Rf is the feedback resistor. Rf and R1 together sets the gain of the amplifier. With the used values of R1 and Rf the gain will be 10 10K/1K = 10). RL is the load resistor and the amplified signal will be available across it. POT R2 can be used for nullifying the output offset voltage. If you are planning to assemble the circuit, the power supply must be well regulated and filtered. Noise from the power supply can

adversely affect the performance of the circuit. When assembling on PCB it is recommended to mount the IC on the board using an IC base.





Observations:

For Gain 1

R_1 =10K , R_2 = 10K

$$[\square\square\square\square = -\frac{\square 2}{\square 1}\square\square\square]$$

Vin	Vout
0V 0.1V 0.3V 0.5V 0.7V 0.9V	

For Gain 10

R_1 =10K , R_2 = 100K

VIN	VOUT
0V 0.1V 0.3V 0.5V 0.7V 0.9V	

In the inverting amplifier only one input is applied and that is to the inverting input ((V2) terminal. The Non inverting input terminal (V1) is grounded. **Since, V1=0 V& V2=Vin Vo= -A Vin**

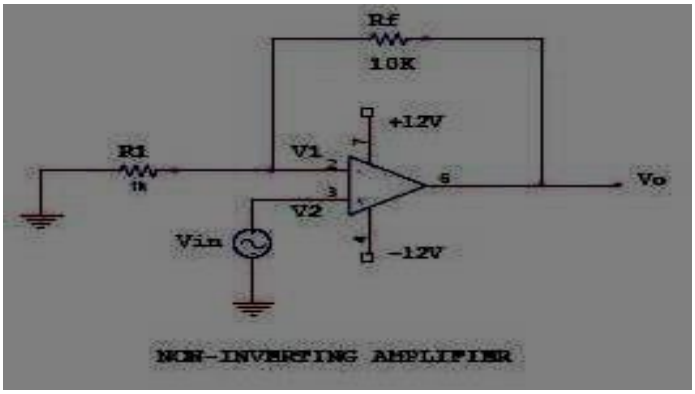
The negative sign indicates the output voltage is 1800 out of phase with respect to the input and amplified by gain A.

Practical Non-inverting amplifier using 741:

The input is applied to the non-inverting input terminal and the Inverting terminal is connected to the ground.

V1= Vin& V2=0Volts Vo= A Vin

The output voltage is larger than he input voltage by gain A & is in phase with the input signal.



Formula- $V_0 = (1+R1/R2)V$

$R^* = \frac{-1 \square 2}{\square 1 + \square 2}$

For Gain 2

$R_1 = 10K$, $R_2 = 10K$

V_{IN}	V_{OUT}
0V 0.1V 0.3V 0.5V 0.7V 0.9V	

For Gain 10

R_1 =10K , R_2 =90K

V_{IN}	V_{OUT}
0V 0.1V 0.3V 0.5V 0.7V 0.9V	

Procedure:

1) Connect the circuit for inverting, non inverting amplifier on a breadboard.
2) Connect the input terminal of the op-amp to function generator and output terminal to CRO.
3) Feed input from function generator and observe the output on CRO.
4) Draw the input and output waveforms on graph paper.

Result: The basic op-amp circuits of inverting & non-inverting amplifiers were designed set up and output waveforms were obtained in a CRO.

The gain obtained are Inverting amplifier: Gain = …….
Non-inverting amplifier: Gain = …….

Precaution:

To ensure stability and prevent oscillations in the amplifier circuit:

- Use op-amps with sufficient bandwidth and slew rate for the desired gain and frequency range.
- Ensure proper decoupling of power supplies to minimize noise and voltage fluctuations.
- Pay attention to the op-amp's input and output capacitance to maintain stability, especially at higher gains and frequencies.

Experiment No 2

Objective: Designing of an analog adder and subtractor Circuits**.**

Digital Adder:

In digital electronics an adder is a logic circuit that implements addition of numbers. In many computers and other types of processors, adders are used to calculate addresses, similar operations and table indices in the arithmetic logic unit (ALU) and also in other parts of the processors. These can be built for many numerical representations like binary coded decimal or excess-3.
Adders are classified into two types:

1. **Half adder**
2. **Full adder**.

Half Adder-

The half adder circuit is required to add two input digits (for Ex. A and B) and generate a carry and sum. The half adder adds two binary digits called as augend and addend and produces two outputs as sum and carry (XOR is applied to both inputs to produce sum and AND gate is applied to both inputs to produce carry). It means half adder circuits can add only two digits in other words if we need to add more than 2 digits it will not work, so, it the limitation of an half adder electronic circuits. To resolve this problem a full adder circuit is required.

Application-

- The ALU of a computer uses half adder to compute the binary addition operation on two bits.
- Half adder is used to make full adder as a full adder requires 3 inputs, the third input being an input carry i.e. we will be able to cascade the carry bit from one adder to the other.
- Ripple carry adder is possible to create a logical circuit using multiple full adders to add N- bit numbers. Each full adder inputs a C (in), which is the C (out) of the previous adder. This kind of adder is called RIPPLE CARRY ADDER, since each carry bit "ripples" to the next full adder.

Full Adder-

A full adder logic circuit has three inputs A, B and C, which add the three input numbers and generate a carry and sum. The full adder adds 3 one bit numbers, where two can be referred to as operands and one can be referred to as bit carried in. And produces 2-bit output, and these can be referred to as output carry and sum. The difference between a half-adder and a full- adder is that the full-adder has three inputs and two outputs, whereas half adder has only two inputs and two outputs. When full-adder logic is designed, you string eight of them together to create a byte-wide adder and cascade the carry bit from one adder to the next. Figure given below show the logic circuits of Half adder and Full adder

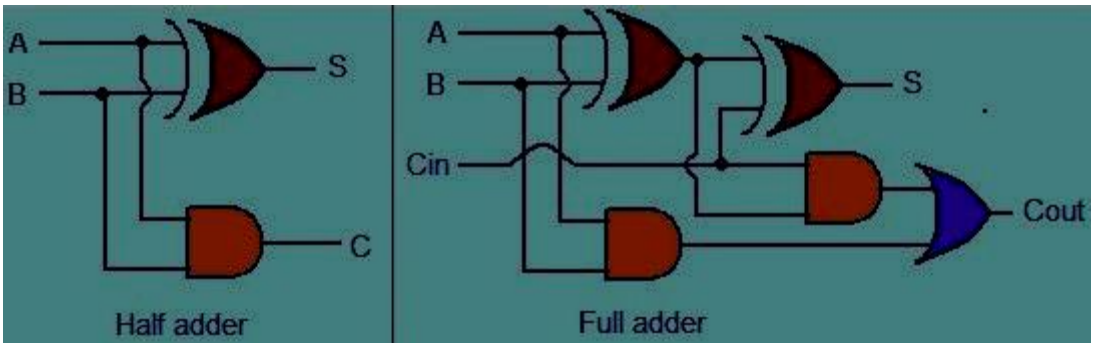
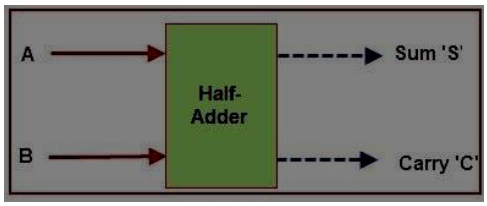


Fig. Half Adder and Full Adder Circuit

Symbol and Operation of Half Adder

Symbol of half adder circuit is shown in figure given below. And the operation can bestated as



You can design simple addition with the help of logic gates for half adder circuits.Let's see an addition of single bits:
0+0 = 0
0+1 = 1
1+0 = 1
1+1 = 10
These are the least possible single-bit combinations. But the result for 1+1 is 10, the sum resultmust be re-written as a 2-bit output. Thus, the equations can be written as
0+0 = 00
0+1 = 01
1+0 = 01
1+1 = 10
The output '1'of '10' is carry-out. 'SUM' is the normal output and 'CARRY' is the carry-out.

Half Adder Truth Table

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

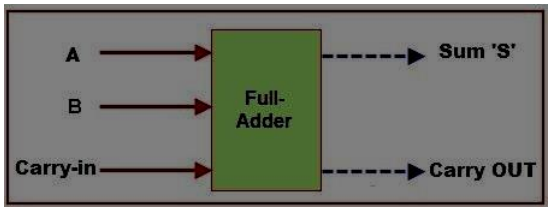
Half Adder Truth Table

Now it is clear that 1-bit adder can be easily implemented with the help of the XOR Gate for the output 'SUM' and an AND Gate for the 'Carry'. When we need to add, two 8-bit bytes together, we can be done with the help of full-adder logic. The half-adder is useful when you want to add one binary digit quantities. A way to develop two-binary digit adders would be to make a truth table and reduce it.

The simplest expression uses the exclusive OR function is:
Sum =A XOR B
Carry A AND B

Full Adder

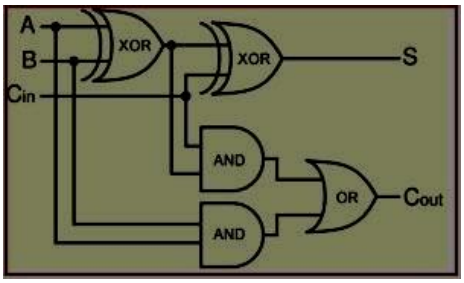
Full adder is difficult to implement than a half adder as it has three inputs. The first two inputs are A and B and the third input is an input carry as C-in. When full adder logic is designed, you string eight of them together to create a byte-wide adder and cascade the carry bit from one adder to the next. The output carry is designated as C OUT and the normal output is designated as S. Logic symbol of full adder circuit is shown below.



Truth Table of full Adder

INPUTS			OUTPUT	
A	B	C-IN	C-OUT	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

With the truth-table, the full adder logic can be implemented. You can see that the output S is an XOR between the input A and the half-adder, SUM output with B and C-IN inputs.
We take C-OUT will only be true if any of the two inputs out of the three are HIGH. So, we can implement a full adder circuit with the help of two half adder circuits. At first, half adder will be used to add A and B to produce a partial Sum and a second half adder logic can be used to add C-IN to the Sum produced by the first half adder to get the final S output.



If any of the half adder logic produces a carry, there will be an output carry. So, C OUT will be an OR function of the half-adder Carry outputs. Take a look at the implementation of the full adder circuit shown below.
The implementation of larger logic diagrams is possible with the above full adder logic a simpler symbol is mostly used to represent the operation. Given below is a simpler schematic representation of a one-bit full adder.

Sum = A XOR B NOT XOR Cin
Carry Out = A.B + Cin (A XOR B)

The relationship between the Full-Adder and the Half-Adder is half adder produces resultsand full adder uses half adder to produce some other result. Similarly, while the Full- Adder is of two Half-Adders, the Full-Adder is the actual block that we use to create the arithmetic circuits.

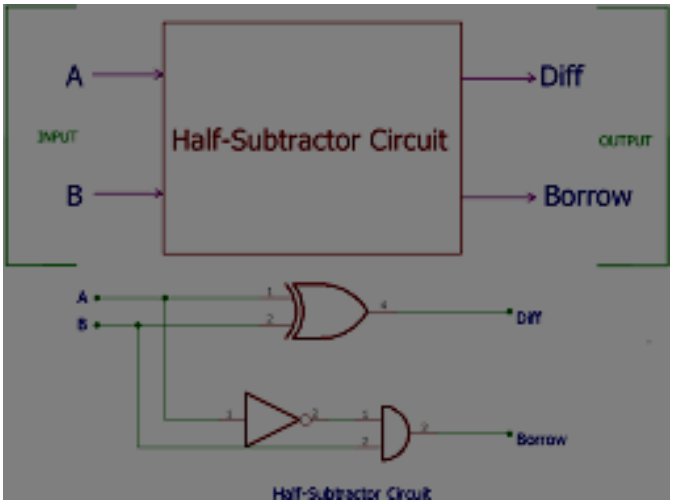
Digital Subtractor

In electronics, a **subtractor** can be designed using the same approach as that of an adder. The binary subtraction process is summarized below. As with an adder, in general case ofcalculations on multi-bit numbers, three bits are involved in performing the subtraction for each bit of the difference: the minuend (**A**), subtrahend (**B**), and a borrow in from the previous (less significant) bit order position ($\mathbf{B_{in}}$). The outputs are the difference bit ($\mathbf{D_{iff}}$) and borrow bit $\mathbf{B_{in}}$+1. The subtractor is best understood by considering that the subtrahend and both borrow bits have negative weights, whereas the **A** and **D** bits are positive.

Half Subtractor-

The half subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, the minuend (**A**) and subtrahend (**B**) and two outputs the difference $\mathbf{D_{iff}}$ and borrows out $\mathbf{B_{out}}$. Borrows out signal is set when the subtractor needs to borrow from the next digit in a multi digit subtraction. That is, $\mathbf{B_{out} = 1}$ when **A** < **B**. Since **A** and **B** are bits, $\mathbf{B_{out} = 1}$ if and only if **A = 0** and **B = 1**. An important point worth mentioning is that the half subtractor diagram aside implements **A - B** and not **B - A** since $\mathbf{B_{out}}$ on the diagram is given by $\mathbf{B_{out}}$ **= NOT A. B**

Figure shown below is depicted the symbol and circuit of a half subtractor.



This is an important distinction to make since subtraction itself is not commutative, but the difference bit $\mathbf{D_{iff}}$ is calculated using an XOR gate which is commutative.

Truth Table

A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Logical Expression:

Difference (**D**) = **A** XOR B
Borrow = NOT **A.B**

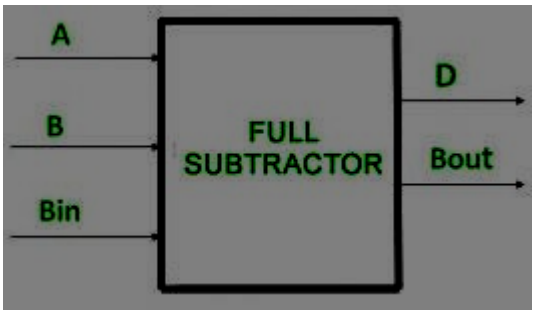
Applications:

- Half subtractor is used to subtract the least significant column numbers. For subtractionof multi-digit numbers, it can be used for the LSB
- Half subtractor is used to reduce the force of audio or radio signals
- It can be used in amplifiers to reduce the sound distortion
- Half subtractor is used in ALU of processor
- It can be used to increase and decrease operators and also calculates the addresses

Full Subtractor

A full subtractor is a combinational circuit that performs subtraction of two bits, one is minuend and other is subtrahend, taking into account borrow of the previous adjacent lower minuend bit. This circuit **has three inputs and two outputs**. The three inputs A, B and Bin, denote the

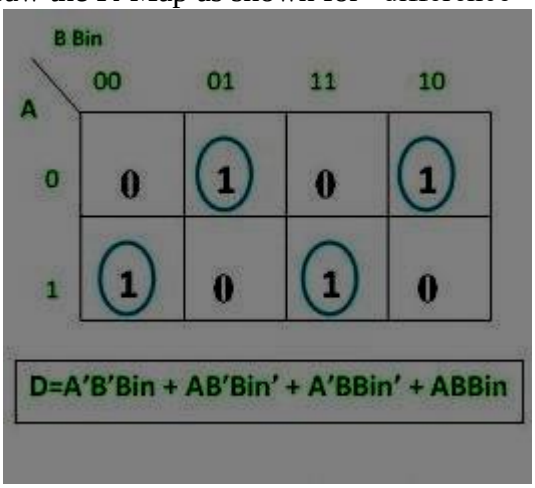
minuend, subtrahend, and previous borrow, respectively. The two outputs, D and Bout represent the difference and output borrows, respectively. Generally, the full subtractor is one of the most used and essential combinational logic circuits. It is a basic electronic device, used to perform subtraction of two binary numbers. Likewise, the full-subtractor uses binary digits like 0, 1 for the subtraction

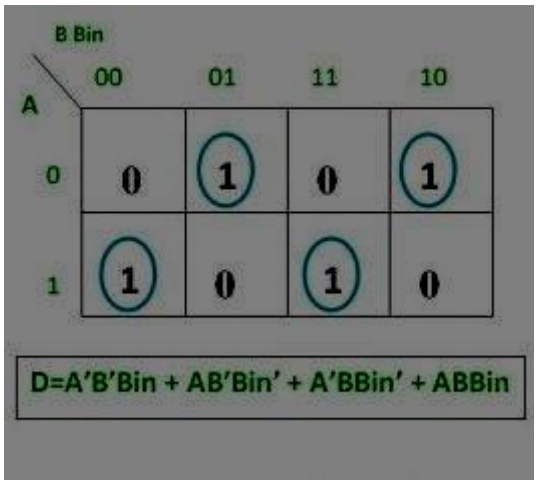


Truth Table

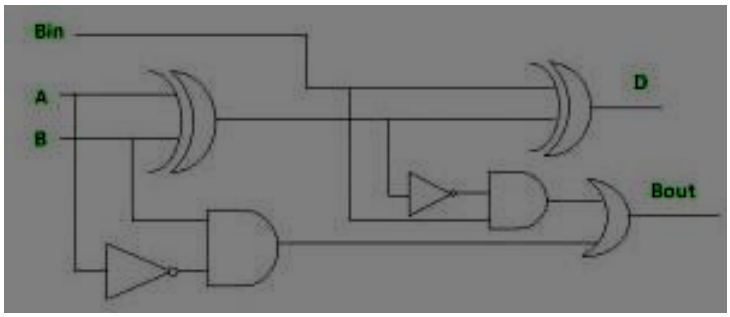
INPUT			OUTPUT	
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

From above table we can draw the K-Map as shown for “difference” and “borrow”.

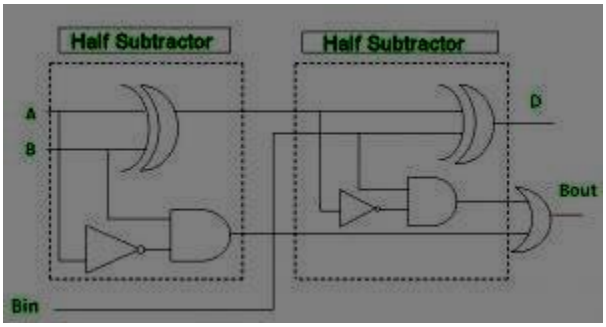




Logic Circuit for Full Subtractor –



Implementation of Full Subtractor using Half Subtractors –2 Half Subtractors and an OR gate is required to implement a Full Subtractor.



Applications

- These are generally employed for ALU in computers to subtract as CPU and GPU for applications of graphics to decrease the circuit difficulty
- Subtractors are mostly used for performing arithmetical functions like subtraction in electronic calculators and digital devices

- These are also applicable for different micro controllers for arithmetic subtraction, timers and program counter (PC)
- Subtractors are used in processors to compute tables, address, etc.

By using any full subtractor logic circuit, full subtractor using NAND gates and full subtractor using NOR gates can be implemented since both the NAND and NOR gates are treated as universal gates.

Experiment No 3

Objective: Designing of an integrator using op-amp for a given specification & study of its frequency response

Apparatus required:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

Theory:

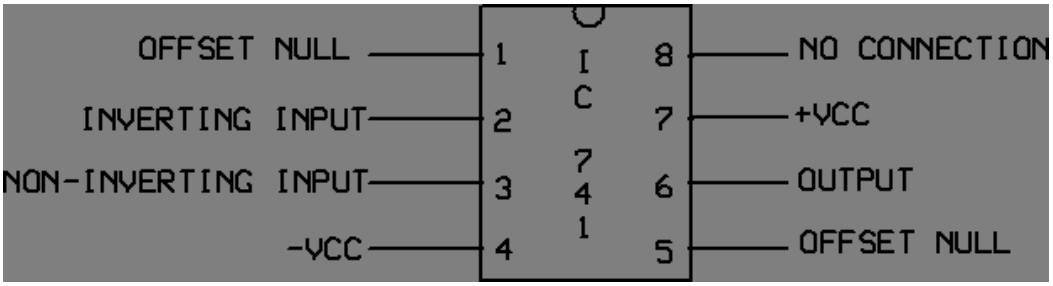
A circuit in which the output voltage waveform is the integral of the input voltage waveform isthe integrator. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_f is replaced by a capacitor C_f . The expression for the output voltage is given as,

$$V_o = - (1/R_f C_1) \int V_i \, dt$$

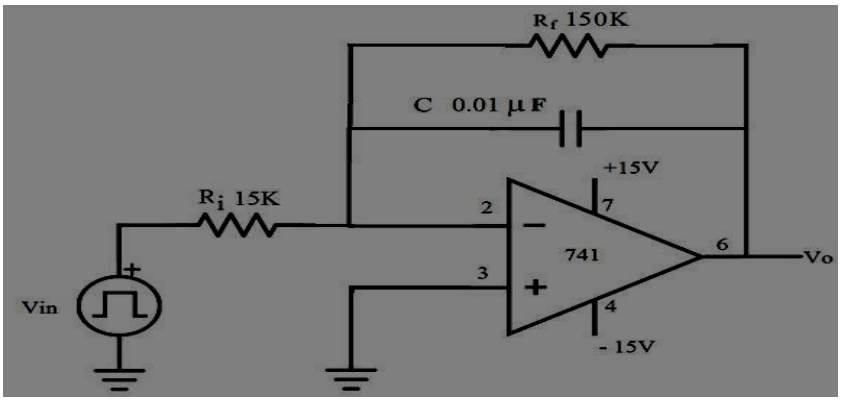
Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. Normally between f_a and f_b the circuit acts as an integrator. Generally, the value of $f_a < f_b$. The input signal will be integrated properly if the Time period T of the signal is larger than orequal to $R_f C_f$. That is, $T \geq R_f C_f$

The integrator is most commonly used in analog computers and ADC and signal-wave shaping circuits.

Pin diagram:



Circuit diagram of integrator:



Design:

Given f =1 KHz So

T = 1/f = 1ms

Design equation is $T = 2\pi R_i C$

Let C = 0.01µF

Then R_i = 15KΩ

Take $R_f = 10R_i$ = 150KΩ

[To obtain the output of an Integrator circuit with component values R_1C_f = 0.1ms , R_f = 10 $R_1$and C_f = 0.01 µF and also if 1 V peak square wave at 1000Hz is applied as input.]

We know the frequency at which the gain is 0 dB, $f_b = 1 / (2\pi R_1 C_f)$
Therefore f_b = _____
Since $f_b = 10 f_a$, and also the gain limiting frequency $f_a = 1 / (2\pi R_f C_f)$
We get , R_1 =_____and hence R_f =_____

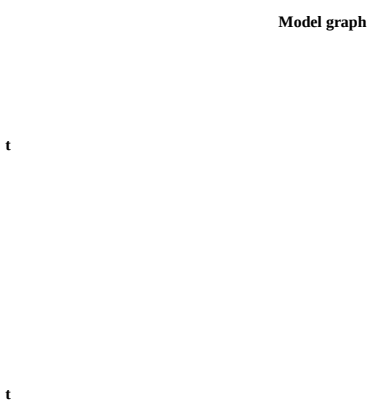
Procedure:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveformsare plotted in a graph sheet.

Observations:

S.No		amplitude	Time period
1.	Sine wave input Cosine wave output		
2.	Square wave input Spike wave output		

Model graph:



Calculation:

Result:

The design of the Integrator circuit was done and the input and output waveforms were obtained**.**

Precaution:

- One important precaution in designing an integrator with an op-amp is to ensure stability, especially at low frequencies where the gain of the integrator becomes very high. To avoid instability issues:
- Use a high-quality op-amp with low input bias current and offset voltage to minimize errors.
- Add a resistor (\(R_f \)) in series with the capacitor (\(C \)) in the feedback loop to improve stability.
- Use a compensation capacitor in parallel with \(R_f \) to limit the integrator's gain at low frequencies and prevent oscillations.
- Consider using a precision capacitor with low temperature coefficient for accurate integration over temperature variations.

Experiment No 4

Objective: Designing of an differentiator using op-amp for a given specification & study of its frequency response.

Apparatus required:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

Theory:

The differentiator circuit performs the mathematical operation of differentiation; that is, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1. The expression for the output voltage is given as,

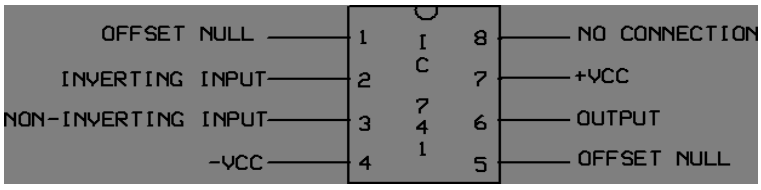
$$V_o = - R_f C_1 (dV_i /dt)$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. A resistor $R_{comp} = R_f$ is normally connected to the non-inverting input terminal of the op- amp to compensate for the input bias current. A workable differentiator can be designed by implementing the following steps:

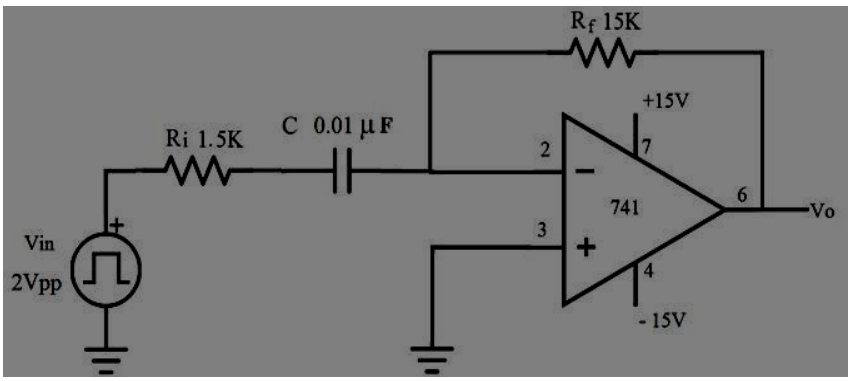
3) Select f_a equal to the highest frequency of the input signal to be differentiated. Then,assuming a value of $C_1 < 1$ µF, calculate the value of R_f.
4) Choose $f_b = 20\ f_a$ and calculate the values of R_1 and C_f so that $R_1C_1 = R_f C_f$.

The differentiator is most commonly used in wave shaping circuits to detect high frequency components in an input signal and also as a rate–of–change detector in FM modulators.

Pin diagram:



Circuit diagram of differentiator:



Design :

Given f = 1 KHzSo

T = 1/f = 1ms

Design equation is $T = 2\pi R_f C$

Let C = 0.01µF

Then $R_f = 15K\Omega$

Let Ri = Rf/10 = 1.5KΩ

[To design a differentiator circuit to differentiate an input signal that varies in frequency from 10 Hz to about 1 KHz. If a sine wave of 1 V peak at 1000Hz is applied to the differentiator , draw its output waveform.]

Given $f_a = 1$ KHz

We know the frequency at which the gain is 0 dB, $f_a = 1 / (2\pi R_f C_1)$Let us assume $C_1 = 0.1$ µF; then

$R_f =$ _____

Since $f_b = 20 f_a$, $f_b = 20$ KHz

We know that the gain limiting frequency $f_b = 1 / (2\pi R_1 C_1)$

Hence $R_1 =$ _____

Also since $R_1C_1 = R_f C_f$; Cf = _____

Given $V_p = 1$ V and f = 1000 Hz, the input voltage is $V_i = V_p \sin \omega t$We know $\omega = 2\pi f$

Hence

$V_o = - R_f C_1 (dV_i / dt)$

$= - 0.94 \cos \omega t$

Procedure:

1. Connections are given as per the circuit diagram.
2. $+ V_{cc}$ and $- V_{cc}$ supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

Observations:

S.No		amplitude	Time period
1.	Sine wave input Cosine wave output		
2.	Square wave input Spike wave output		

Calculation:

Result:

The design of the Differentiator circuit was done and the input and output waveforms were obtained.

Precautions:

- Ensure that the op-amp is powered within its specified voltage range to avoid damage.
- Use decoupling capacitors at the power supply pins of the op-amp to filter out high-frequency noise.
- Ensure proper grounding and layout to minimize noise and signal interference.
- Check the maximum input voltage allowed by the op-amp to avoid saturation or clipping.

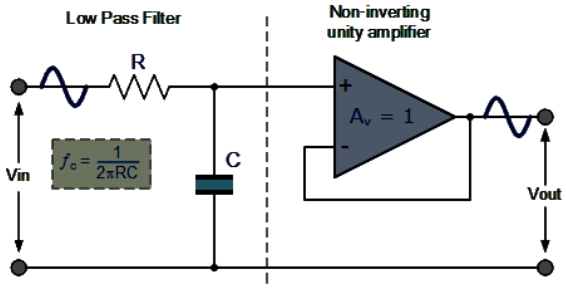
Experiment No 5

Objective: Designing a first order Low-pass filter using op-amp.

Theory: Active filters such as an active low pass filter, are filter circuits that use an operational amplifier (op-amp) as the their main amplifying device along with some resistors and capacitors to provide a filter like performance at low frequencies.
Basic first-order passive filter circuits, such as a low pass or a high pass filter can be constructed using just a single resistor in series with a non-polarized capacitor connected across a sinusoidal input signal. The main disadvantage of passive filters is that the amplitude of the output signal is less than that of the input signal, ie, the gain is never greater than unity and that the load impedance affects the filters characteristics. With passive filter circuits containing multiple stages, this loss in signal amplitude called "Attenuation" can become quiet severe. One way of restoring or controlling this loss of signal is by using amplification through the use of **Active Filters**. As their name implies, Active Filters contain active components such as operational amplifiers, transistors or FET's within their circuit design. They draw their power from an external power source and use it to boost or amplify the output signal.

A first-order (single-pole) **Active High Pass Filter** as its name implies, attenuateslow frequencies and passes high frequency signals. It consists simply of a passive filter section followed by a non-inverting operational amplifier. The frequency response of the circuit is the same as that of the passive filter, except that the amplitude of the signal is increased by the gain of the amplifier and for a non-inverting amplifier the value of the pass band voltage gain is given as 1 + R2/R1, the same as for the low pass filter circuit

First Order Low Pass Filter:



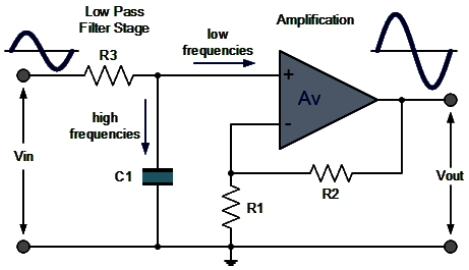
The first-order low pass active filter, consists simply of a passive RC filter stage providing a low frequency path to the input of a non-inverting operational amplifier. The amplifier is configured as a voltage-follower (Buffer) giving it a DC gain of one, Av = +1 or unity gain as opposed to the previous passive RC filter which has a DC gain of less than unity.

The advantage of this configuration is that the op-amps high input impedance prevents excessive loading on the filters output while its low output impedance prevents the filters cut-off frequency point from being affected by changes in the impedance of the load.

While this configuration provides good stability to the filter, its main disadvantage is that it has no voltage gain above one. However, although the voltage gain is unity the power gain is very high as its

output impedance is much lower than its input impedance. If a voltage gain greater than one is required we can use the following filter circuit.

Active Low Pass Filter with Amplification:



The frequency response of the circuit will be the same as that for the passive RC filter, except that the amplitude of the output is increased by the pass band gain, AF of the amplifier. For a non-inverting amplifier circuit, the magnitude of the voltage gain for the filter is given as a function of the feedback resistor (R2) divided by its corresponding input resistor (R1) value and is given as:

$$\text{DC gain} = \left(1 + \frac{R_2}{R_1}\right)$$

Therefore, the gain of an active low pass filter as a function of frequency will be

Gain of a first-order low pass filter

$$\textit{Voltage Gain, } (Av) = \frac{Vout}{Vin} = \frac{A_F}{\sqrt{1 + \left(\frac{f}{fc}\right)^2}}$$

Where:

- AF = the pass band gain of the filter, (1 + R2/R1)
- f = the frequency of the input signal in Hertz, (Hz)
- fc = the cut-off frequency in Hertz, (Hz)

Thus, the operation of a low pass active filter can be verified from the frequency gain equation above as:

1. At very low frequencies, $f < f$c $\quad \frac{Vout}{Vin} \cong A_F$

2. At the cut-off frequency, $f = f$c $\quad \frac{Vout}{Vin} = \frac{A_F}{\sqrt{2}} = 0.707 A_F$

3. At very high frequencies, $f > f$c $\quad \frac{Vout}{Vin} < A_F$

Thus, the **Active Low Pass Filter** has a constant gain AF from 0Hz to the high frequency cut-off point, fC. At fC the gain is 0.707AF, and after fC it decreases at a constant rate as the frequency increases. That is, when the frequency is increased tenfold (one decade), the voltage gain is divided by 10.

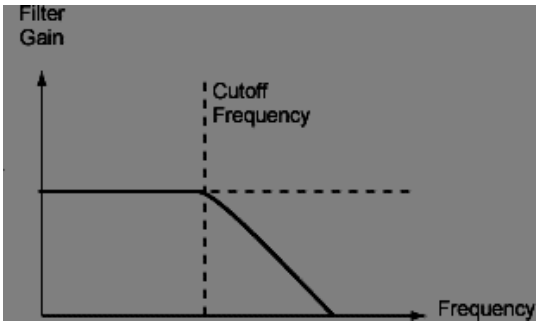
In other words, the gain decreases 20dB (= 20*log(10)) each time the frequency is increased by 10. When dealing with filter circuits the magnitude of the pass band gain of the circuit is generally expressed in decibels or dB as a function of the voltage gain, and this is defined as:

Magnitude of Voltage Gain in (dB)

$$\mathrm{Av(dB)} = 20\log_{10}\left(\frac{\mathrm{Vout}}{\mathrm{Vin}}\right)$$

$$\therefore\ -3\mathrm{dB} = 20\log_{10}\left(0.707\,\frac{\mathrm{Vout}}{\mathrm{Vin}}\right)$$

Model graph:



Procedure :

1. Design the circuit for the given value of closed llop gfain and cutoff frequency.

2. Fix the input signal voltage and measure the peak to peak output voltage for a different frequency.

3. plot the frequency response (gain=$20\log_{10}$ (v_o/v_i) Vs input signal frequency) and find the 3 dB frequency from here.

4. Compare the theoritical and practical values of the closed loop gain and cutoff frequency.

Table:

SI. No.	Input signal frequency	V_o(volts)	Gain (dB)

	(Hz)		

Results:

Precautions:

1. External connections to OP-AMP should be made to correct [in.

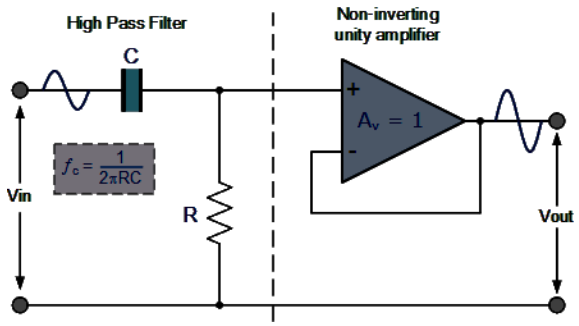
2. Various voltages applied to the pins of OP-AMP should not exceed the rated value.

Experiment No 6

Objective: Designing a first order High-pass filter using op-amp.

Theory: A first-order (single-pole) **Active High Pass Filter** as its name implies, attenuateslow frequencies and passes high frequency signals. It consists simply of a passive filter section followed by a non-inverting operational amplifier. The frequency response of the circuit is the same as that of the passive filter, except that the amplitude of the signal is increased by the gain of the amplifier and for a non-inverting amplifier the value of the pass band voltage gain is given as 1 + R2/R1, the same as for the low pass filter circuit.

First Order High Pass Filter

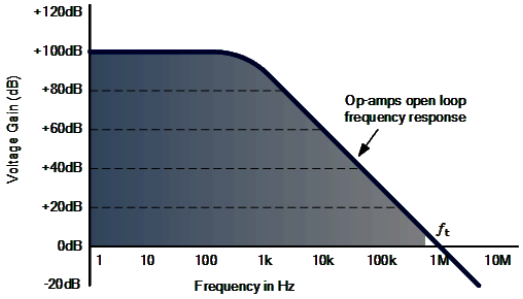


Technically, there is no such thing as an active high pass filter. Unlike Passive High Pass Filters which have an "infinite" frequency response, the maximum pass band frequency response of an active high pass filter is limited by the open-loop characteristics or bandwidth of the operational amplifier being used, making them appear as if they are band pass filters with a high frequency cut-off determined by the selection of op-amp and gain.

In the Operational Amplifier tutorial we saw that the maximum frequency response of an op-amp is limited to the Gain/Bandwidth product or open loop voltage gain (AV) of the operational amplifier being used giving it a bandwidth limitation, where the closed loop response of the op amp intersects the open loop response.

A commonly available operational amplifier such as the uA741 has a typical "open-loop" (without any feedback) DC voltage gain of about 100dB maximum reducing at a roll off rate of -20dB/Decade (-6db/Octave) as the input frequency increases. The gain of the uA741 reduces until it reaches unity gain, (0dB) or its "transition frequency" (ft) which is about 1MHz. This causes the op-amp to have a frequency response curve very similar to that of a first-order low pass filter and this is shown below.

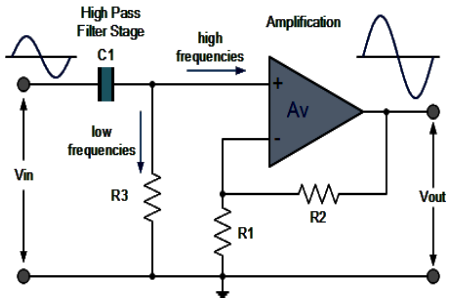
Frequency response curve of a typical Operational Amplifier



Then the performance of a "high pass filter" at high frequencies is limited by this unity gain crossover frequency which determines the overall bandwidth of the open-loop amplifier. The gain-bandwidth product of the op-amp starts from around 100kHz for small signal amplifiers up to about 1GHz for high-speed digital video amplifiers and op-amp based active filters can achieve very good accuracy and performance provided that low tolerance resistors and capacitors are used.

Under normal circumstances the maximum pass band required for a closed loop active high pass or band pass filter is well below that of the maximum open-loop transition frequency. However, when designing active filter circuits it is important to choose the correct op-amp for the circuit as the loss of high frequency signals may result in signal distortion.

Active High Pass Filter with Amplification



This first-order high pass filter, consists simply of a passive filter followed by a non-inverting amplifier. The frequency response of the circuit is the same as that of the passive filter, except that the amplitude of the signal is increased by the gain of the amplifier.

For a non-inverting amplifier circuit, the magnitude of the voltage gain for the filter is given as a function of the feedback resistor (R2) divided by its corresponding input resistor (R1) value and given as

Gain for an Active High Pass Filter

$$\text{Voltage Gain, (Av)} = \frac{\text{Vout}}{\text{Vin}} = \frac{A_F\left(\frac{f}{fc}\right)}{\sqrt{1+\left(\frac{f}{fc}\right)^2}}$$

Where:

- AF= the Pass band Gain of the filter, (1 + R2/R1)
- f= the Frequency of the Input Signal in Hertz, (Hz)
- fc= the Cut-off Frequency in Hertz, (Hz)

Just like the low pass filter, the operation of a high pass active filter can be verified from the frequency gain equation above as:

1. At very low frequencies, $f < fc$ $\frac{Vout}{Vin} < A_F$

2. At the cut-off frequency, $f = fc$ $\frac{Vout}{Vin} = \frac{A_F}{\sqrt{2}} = 0.707 A_F$

3. At very high frequencies, $f > fc$ $\frac{Vout}{Vin} \cong A_F$

Then, the **Active High Pass Filter** has a gain AF that increases from 0Hz to the low frequency cut-off point, fC at 20dB/decade as the frequency increases. At fC the gain is 0.707*AF, and after fC all frequencies are pass band frequencies so the filter has a constant gain AF with the highest frequency being determined by the closed loop bandwidth of the op-amp

When dealing with filter circuits the magnitude of the pass band gain of the circuit is generally expressed in *decibels* or *dB* as a function of the voltage gain, and this is defined as:

Magnitude of Voltage Gain in (dB)

$$Av(dB) = 20\log_{10}\left(\frac{Vout}{Vin}\right)$$

$$\therefore -3dB = 20\log_{10}\left(0.707\frac{Vout}{Vin}\right)$$

For a first-order filter the frequency response curve of the filter increases by 20dB/decade or 6dB/octave up to the determined cut-off frequency point which is always at -3dB below the maximum gain value. As with the previous filter circuits, the lower cut-off or corner frequency (fc) can be found by using the same formula:

$$fc = \frac{1}{2\pi RC}\ Hz$$

The corresponding phase angle or phase shift of the output signal is the same as that given for the passive RC filter and leads that of the input signal. It is equal to +45o at the cut-off frequency fc value and is given as:

$$Phase\ Shift\ \phi = tan^{-1}\left(\frac{1}{2\pi fRC}\right)$$

A simple first-order active high pass filter can also be made using an inverting operational amplifier configuration as well, and an example of this circuit design is given along with its corresponding frequency response curve. A gain of 40dB has been assumed for the circuit.

Procedure:

1. Connect the circuit as shown in the diagram.
2. Connect the DSO to the probes and switch it on.
3. Check the graph for the both positive and negative voltage and write down the output.

Tabulation:

INPUT FREQUENCY(HZ)	OUTPUT VOLTAGE(V)	GAIN	GAIN IN db

Results:

Precautions:

1. External connections to OP-AMP should be made to correct [in.

2. Various voltages applied to the pins of OP-AMP should not exceed the rated value.

Experiment No 7

Objective: Designing of a RC Phase shift oscillator using op-amp.

Theory: The basic RC Oscillator which is also known as a Phase-shift Oscillator, produces a sine wave output signal using regenerative feedback obtained from the resistor- capacitor combination. This regenerative feedback from the RC network is due to the ability of the capacitor to store an electric charge. This resistor-capacitor feedback network can be connected to produce a leading phase shift (phase advance network) or interchanged to produce a lagging phase shift (phase retard network) the outcome is still the same as the sine wave oscillations only occur at the frequency at which the overall phase-shift is 360^o. By varying one or more of the resistors or capacitors in the phase-shift network, the frequency can be varied and generally this is done by keeping the resistors the same and using a 3-ganged variable capacitor. In a Resistance-Capacitance Oscillator or simply an RC Oscillator, we make use of the fact that a phase shift occurs between the input to a RC network and the output from the same network by using RC elements in the feedback branch, for example. RC Phase-Shift Network: The circuit on the left shows a single resistor-capacitor network whose output voltage "leads" the input voltage by some angle less than 90^o. An ideal single-pole RC circuit would produce a phase shift of exactly 90^o, and because 180^o of phase shift is required for oscillation, at least two

single-poles must be used in an *RC oscillator* design.

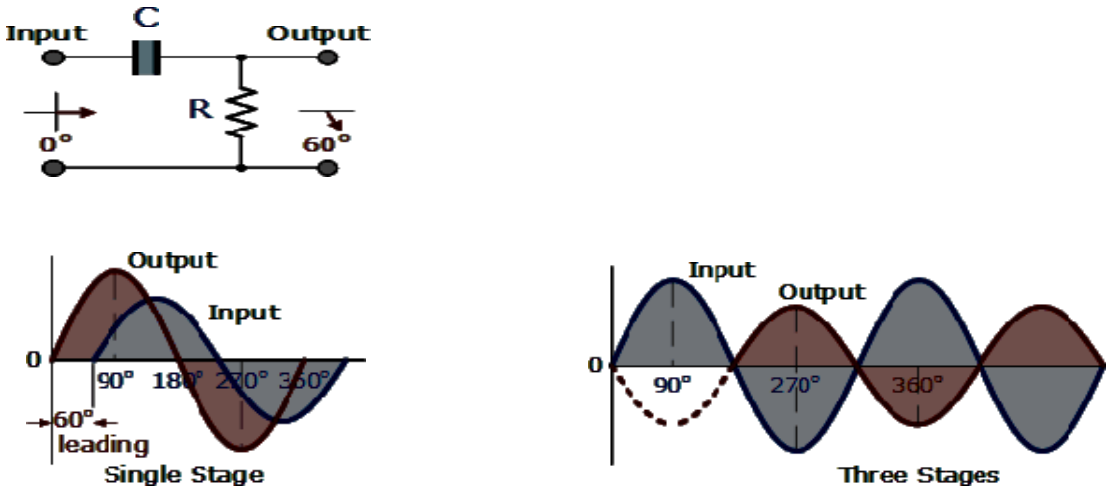


Fig.1: Phase Shift Network

Circuit Diagram:

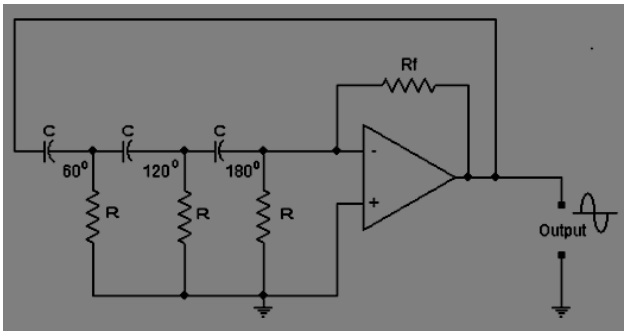


Figure 2: RC phase shift Oscillator using Op-amp

Procedure:

1) Construct the RC phase circuit on the breadboard as shown in the circuit diagram.
2) Use: V_{++} = 14 V, V_{--} = -14 V, R_i = 10kΩ, and R_f = 470kΩ.
3) Capacitor value is 0.0022 uF.
4) Find f_c practically and theoretically.

Theoretical Frequency Calculation:

$$f_c = \frac{1}{2\pi RC\sqrt{6}} = \frac{1}{2\pi\,(10\,K)(0.0022\,uF)\sqrt{6}} = 2.95\,kHz$$

Observations Graph:

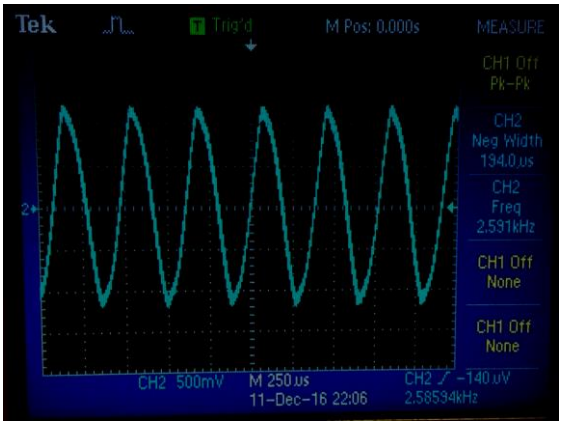


Fig 3: Output Wave with a Frequency =2.589KHz

Table1.: Theoretical and Practical Frequencies of RCphase shift Oscillator

Observations	
Theoretical Frequency of the Oscillator	**=2.95KHz**
Practical Frequency of the Oscillator	**=2.589KHz**

Practical Frequency generated by RC Phase Shift Oscillator is f_c=2.589KHz

Conclusion:

The practical circuit of RC phase shift oscillator is successfully conducted, it has generated a sine wave of frequency f_c=2.589KHz, with an amplitude of

500mVX4.75=2.375 Volts

The error percentage is 11 %.

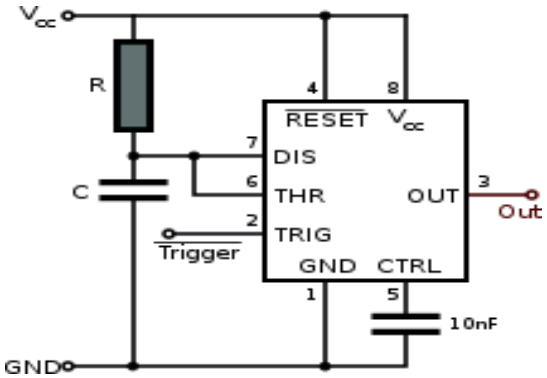
Experiment No 8

Objective: Study of IC 555 as an astable multivibrator.

Theory: In the 555 Oscillator above, pin 2 and pin 6 are connected together allowing the circuit to retrigger itself on each and every cycle allowing it to operate as a free running oscillator. During each cycle capacitor, C charges up through both timing resistors, R1 and R2 but discharges itself only through resistor, R2 as the other side of R2 is connected to the discharge terminal, pin 7. Then the capacitor charges up to 2/3Vcc (the upper comparator limit) which is determined by the 0.693(R1+R2)C combination and discharges itself down to 1/3Vcc (the lower comparator limit) determined by the 0.693(R2.C) combination. This results in an output waveform whose voltage level is approximately equal to Vcc - 1.5V and whose output "ON" and "OFF" time periods are determined by the capacitor and resistors combinations. The individual times required completing one charge and discharge cycle of the output is therefore given as:

$t_1 = 0.693\ (R1+R2)C$, $t_2 = 0.693\ R2C$, $T = t_1 + t_2$

Circuit Diagram:



Procedure:

1. Connect the circuit as shown in the figur.
2. Use potentiometer in case output is not proper.

Observation:

Trace the output waveform and calculate the frequency from the fundamental period of the wave.

Result & Discussion: The waveform was traced and compared with the designed theoretical one.

Experiment No 9

Objective: Study of IC 555 as an monostable multivibrator .

Theory: It has one stable and one quasi stable state. The circuit is useful for generating single output pulse of time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The diode gives a negative triggering pulse. When the output is +Vsat, a diode clamps the capacitor voltage to 0.7V then, a negative going triggering impulse magnitude Vi passing through RC and the negative triggering pulse is applied to the positive terminal. Let us assume that the circuit is instable state. The output V0i is at +Vsat. The diode D1 conducts and Vc the voltage across the capacitor 'C' gets clamped to 0.7V,the voltage at the positive input terminal through R1R2 potentiometer divider is +ßVsat. Now, if a negative trigger of magnitude Vi is applied to the positive terminal so that the effective signal is less than 0.7V.the output of the Op-Amp will switch from +Vsat to –Vsat. The diode will now get reverse biased and the capacitor starts charging exponentially to –Vsat. When the capacitor charge Vc becomes slightly more negative than –ßVsat, the output of the op-ampswitches back to +Vsat. The capacitor 'C' now starts charging to +Vsat through R until Vc is 0.7V.

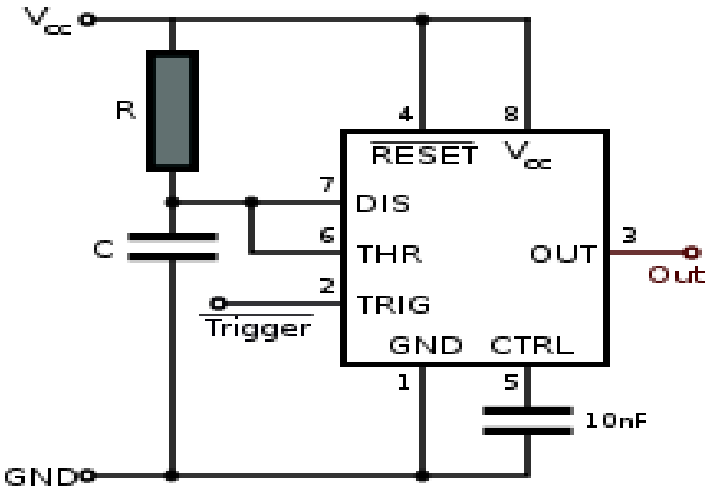
$V0 = Vf + (Vi-Vf)$ □□/□□

ß = R2/(R1+R2)If Vsat >> Vp

and R1=R2 and ß = 0.5,

Then, T= 0.69RC

Circuit Diagram:



Procedure:

1. Connect the circuit as shown in the circuit diagram.
2. Apply Negative triggering pulses at pin 2 of frequency 1 KHz as shown in Fig.
3. Observe the output waveform and capacitor voltage as shown in Figure and measure the pulse duration.
4. Theoretically calculate the pulse duration as $T_{high} = 1.1\ RC$
5. Compare it with experimental values.

Observation: Trace the time period of the output wave form and compare it with the given one.

Result & Discussion: The waveform is observed and verified with stated condition.