“SEMICONDUCTOR PHYSICS & DEVICES LABORATORY MANUAL”

B.Sc. ELECTRONICS II SEMESTER

MAJOR II

Course Code: PLUBTL1

DEPARTMENT OF PURE AND APPLIED PHYSICS

GURU GHASIDAS VISHWAVIDYALAYA, BILASPUR (C.G)

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Semiconductor Physics & Devices Laboratory Manual

B.Sc. Electronics IInd Semester Major II

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Experiment List

1. Study of the I-V Characteristics of PN Diode.
2. Study of I-V characteristics of Zener Diode.
3. Study of the I-V Characteristics of the Common Emitter Configuration of BJT and to obtain r_i, r_0, β.
4. Study of the I-V Characteristics of the Common Base Configuration of BJT and to obtain r_i, r_0, α.
5. Study of the I-V Characteristics of the Common Collector Configuration of BJT and to obtain voltage gain, r_i, r_0.
6. Study of the I-V Characteristics of UJT.
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Department of Pure & Applied Physics

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Experiment 1: Study of the I-V Characteristics of PN Diode

Objective: To plot forward and reverse I-V characteristics of a given PN junction diode and to determine the static resistance of the given diode

Apparatus: Semiconductor P-N junction diode kit and connecting wires.

Theory:

Semiconductors, like Silicon or Germanium, are elements having resistivity that in intermediate between a conductor and an insulator. They inherently have four electrons in the valence band which helps them to form covalent bonds with four neighbouring silicon atoms. Hence, at absolute zero, the material behaves like an insulator. At room temperature, few of these electrons absorb enough energy to break away from the nucleus and serve as conduction electrons. The conduction properties can also be easily changed by changing the doping (adding different elements to) the semiconductor. Addition of a pentavalent impurity such as Phosphorus, N – type dopant, gives an additional electron after the four silicon bonds are satisfied. Similarly, a trivalent impurity such as Boron, P-type dopant, creates an absence of electron, a hole. The entire semiconductor diode is prepared through a metallurgical junction between the P and N regions of a semiconducting material such as germanium or silicon and it is a single crystal, with one region with excess holes (P-type), and the adjacent region to be N- type, with excess electrons. This creates. The contact to the P region is called the anode and that of the N region is called cathode. Holes and electrons are respectively the charge carriers in P and N type and these are majority charge carriers.

A large density gradient in both hole and electron concentrations occur at this junction. Initially, then, there is a diffusion of holes from the P region to the N region and diffusion of electrons from N region to the P region. The flow of holes from P region uncovers negatively charged acceptor ions, and the flow of electrons uncovers positively charged donor ions. This action creates a charge separation which sets up an electric field oriented in the direction from the positive to the negative charge. This sets up an electric field in such a direction as to oppose the movement of electrons and holes eventually. The region surrounding the junction which contains immobile charges is called the "space charge" or "depletion" region. In this process (+)ve charge gets accumulated at the barrier of N region and (-)ve charge at the barrier of the P region, creating a potential barrier corresponding to the oppose electric field across the depletion region, which is called the built-in potential barrier. This is about 0.7 V for a Si diode at room temperature.

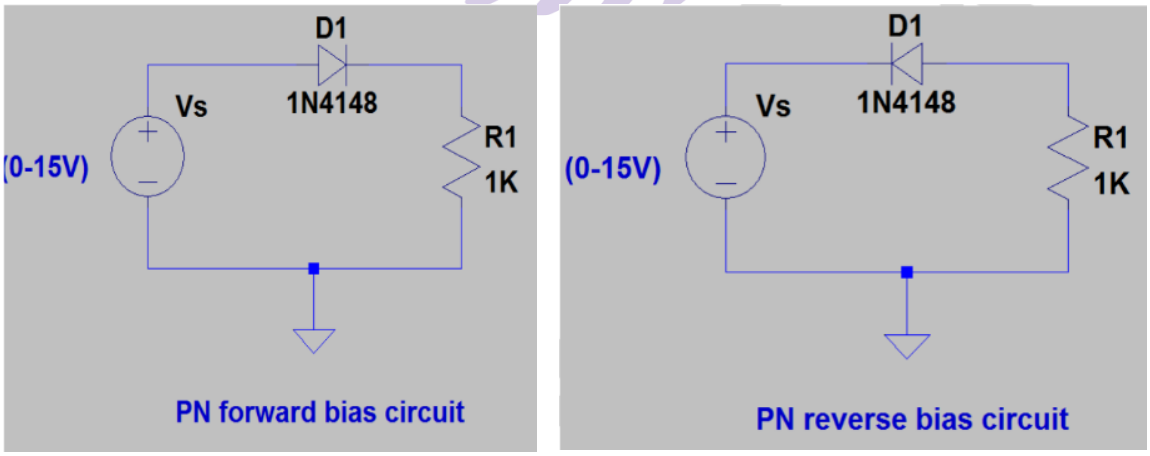
Forward biasing:

When anode of an external battery is connected to the P side and cathode to the N side, it is called Forward biasing. Application of a positive voltage to the P region and negative voltage to the N region creates an additional electric field in the space charge region. But this time the field opposes the space-charge E-field. This disturbs the balance between diffusion and E-field force. When the applied potential is lower than the barrier potential, negligible current flow through the junction. As the applied potential became higher than that of the barrier potential, majority carriers (holes) from the P region diffuse over to the N side and electrons from N side move over to the P side of the junction. This process continues as long as the voltage is applied and the current start flowing through the junction at the external circuit. The voltage at which current start increasing is called 'Knee voltage'. Thus, in the forward bias mode, the forward current is increases with the applied potential difference and the diode carries a large current.

Reverse biasing:

When anode of an external battery is connected to the N side and cathode to the P side, it is called Reverse biasing. In this case, the polarity of the fictious battery in the depletion region is the same as that of the external battery and this leads to the increase in the electric field (potential barrier) holds back the holes in the P region and electrons in the N region and hence, there is hardly any current flowing in the external circuit as both the majority charge carriers drawn away from the junction. However, small reverse current which flows through the junction is due to the minority carriers i.e. electrons in P region and holes in N region. The minority carriers are generated due to the action of light and thermal agitation. Thus, the electric field and the width of the space-charge region increases. There is also a decrease in junction capacitance associated due to increase in the width. Thus, the reverse bias region is characterized by negligible current (due to minority carriers) even on the application of a very high voltage across the terminals, the limit being decided by 'Reverse Breakdown Voltage' of the diode and it is defined as the certain critical limit beyond which if the potential difference in the reverse direction is increased, then simultaneously the reverse current abruptly increases causing 'Avalanche Breakdown'. So a PN diode offers a negligible resistance when forward biased and a very high resistance when reverse biased.

Circuit Diagram:



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Experimental Procedure:

Forward Bias Characteristics:

1. Make Circuit according to the diagram by connecting the wires (use 1V range for voltmeter and 1 mA range for ammeter).
2. By increasing the voltage across the diode in steps of 0.1 volts and note down corresponding current in Table: 1.
3. Calculate static resistance using the forward bias curve, take the points on the curve beyond knee voltage and calculate R_{static} = potential at a point beyond the Knee voltage/current at that point.

Reverse Bias Characteristics:

1. Make Circuit according to the diagram by connecting the wires (use 10V range for voltmeter and 50 μA range for ammeter).
2. By increasing the voltage across the diode in steps of 1.0 volts and note down corresponding current in Table: 2.
3. Calculate static resistance using the forward bias curve, take the points on the curve beyond knee voltage and calculate R_{static} = potential at a point beyond the Knee voltage/current at that point.
4. From this graph, calculate the forward resistance by calculation the slope of the curve in the ON region (where there is sufficiently large change in current w.r.t voltage). If measured slope is m, then Forward resistance: $r_{ON} = 1/m$

Observation Table:

Table:1 (for Forward Bias Characteristics)

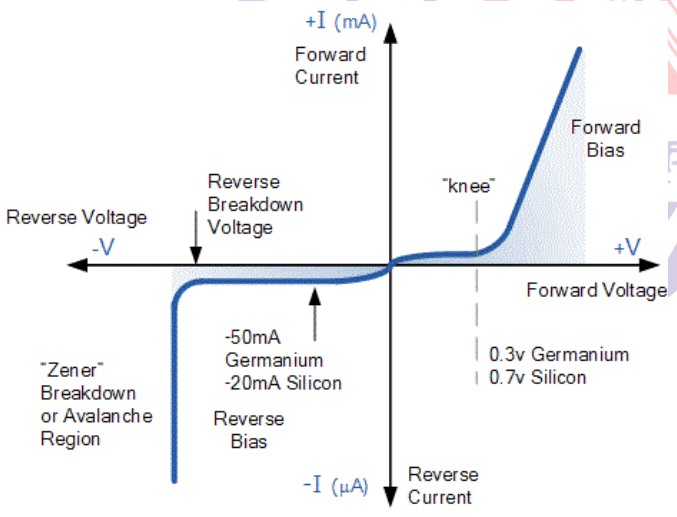
S. No.	Voltage (volts)	Current (mA)
1		
2		
3		
4		

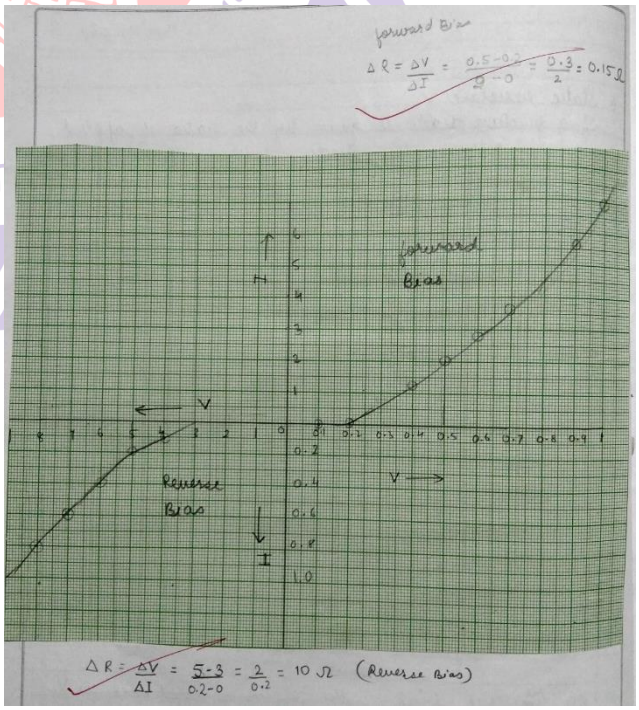
5		
6		
7		
8		
9		
10		

Table:2 (for Reverse Bias Characteristics)

S. No.	Voltage (volts)	Current (μA)
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		

Model graph:





Calculation:

Calculate dynamic resistance and cut-in voltage from graph for the given diode.

Results:

a. Forward Bias of PN Junction Diode:

The Cut in Voltage or Knee Voltage: _____Volts.

The Dynamic Forward resistance: _____ Ohms.

b. Reverse Bias of PN Junction Diode:

The Dynamic Reverse resistance: _____ Ohms.

The Static Reverse resistance: _____ Ohms.

Precautions:

1. Voltmeter and ammeter of appropriate ranges should be selected.
2. The variation in V should be done in steps of 0.1 V in Forward bias.
3. The Battery connections of PN junction diode should be checked and it should be ensured that P is connected to positive and N to the negative of the battery in forward bias.
4. Never cross the limits specified by the manufacturer, otherwise the diode will get damaged.

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Experiment 2: Study of I-V Characteristics of Zener Diode

Objective:

1. Study I-V characteristics of a given Zener diode and to determine the breakdown voltage of the given diode.
2. To study Zener diode as voltage regulator.
3. To calculate % line and load regulation.

Apparatus: Zener diode (6.8V, 1A), Bread board, Resistor (1KΩ, 100Ω), Connecting wires, Voltmeter (0-10 V, 0-30V), Ammeters (0-10mA, 0-1 mA, 0-500 μ A), DC power supply (0-30V), 10KΩ pot and multimeter.

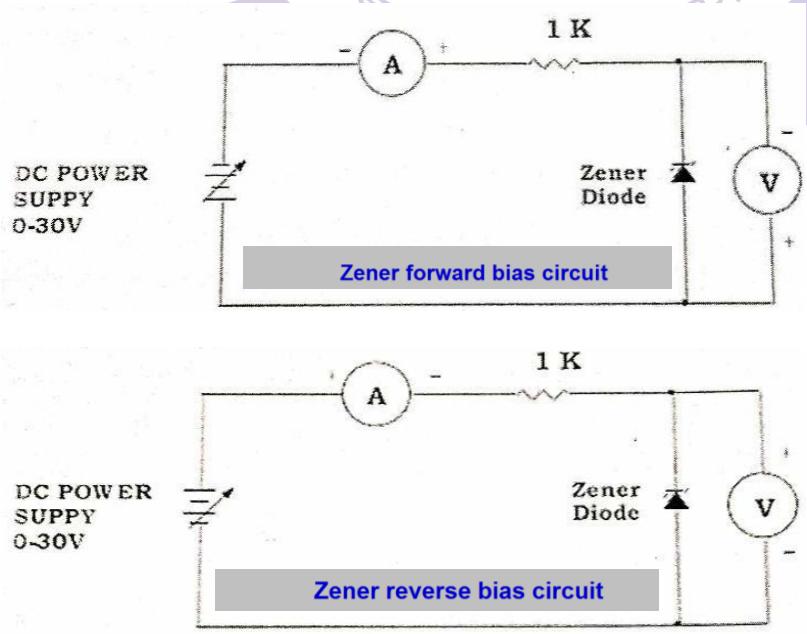
Theory:

Zener diode is a P-N junction diode specially designed with a heavily doped Silicon diode to operate in the reverse biased mode. It is acting as normal diode while forward biasing. It has a particular voltage known as break down voltage, at which the diode break downs while reverse biased. In the case of normal diodes the diode damages at the break down voltage. But Zener diode is specially designed to operate in the reverse breakdown region. The basic principle of Zener diode is the Zener breakdown. When a diode is heavily doped, it's depletion region will be narrow. When a high reverse voltage is applied across the junction, there will be very strong electric field at the junction at a small voltage producing large number of charge carriers (electron hole pair) by breaking the covalent bonds. Thus, heavy current flows due to the sudden increase in charge carriers. This is known as Zener breakdown. The breakdown voltage depends upon the

amount of doping. For a heavily doped diode depletion layer will be thin and breakdown occurs at low reverse voltage and the breakdown voltage is sharp, whereas a lightly doped diode has a higher breakdown voltage. This explains the Zener diode characteristics in the reverse bias region. So, a Zener diode, in a forward biased condition acts as a normal diode. In reverse biased mode, after the break down of junction current through diode increases sharply. But the voltage across it remains constant. This principle is used in voltage regulator using Zener diodes.

Generally, The relation between I-V is almost linear in this case $V_z = V_{z0} + I_z r_z$, where r_z is the dynamic resistance of the Zener at the operating point. V_{z0} is the voltage at which the straight-line approximation of the I-V characteristic intersects the horizontal axis. After reaching a certain voltage, called the breakdown voltage, the current increases widely even for a small change in voltage. However, there is no appreciable change in voltage. So, when we plot the graph, we should get a curve very near to x-axis and almost parallel to it for quite sometimes. After the Zener potential V_z there will be a sudden change and the graph will become exponential.

Circuit Diagram:



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Zener diode as Voltage regulator:

Voltage regulator is nothing but an electronic circuit which keeps o/p voltage constant irrespective of changes in line voltage & load current. The voltage regulator consisting of Zener diode is shown in Fig. 1 and it consists of a current limiting resistor R_{IN} connected in series with the input voltage V_{IN} and Zener diode is connected in parallel with the load R_L in reverse biased condition. The input voltage should be greater than V_Z, then only Zener diode will work in Zener region. The output voltage is always selected with a breakdown voltage V_Z of the diode. If V_{IN} is higher than V_Z the current through Zener diode increases & I_L we will get constant o/p voltage. If I_L changes, then I_Z changes in such a way that at the o/p we get constant dc voltage.

The current flowing through the Zener diode increases to the maximum circuit value (I) determined by: $I = (V_{in} - V_Z) / R_{IN}$; where I is the sum of the Zener current I_Z and the load current I_L. The voltage across the Zener diode becomes stable and is called the "zener voltage", (V_Z), which is for example, 5.1V or 6.2V. This Zener breakdown voltage on the I-V curve is almost a vertical straight line. However, when the input voltage increases, the current I_Z increases causing a decrease in the output voltage.

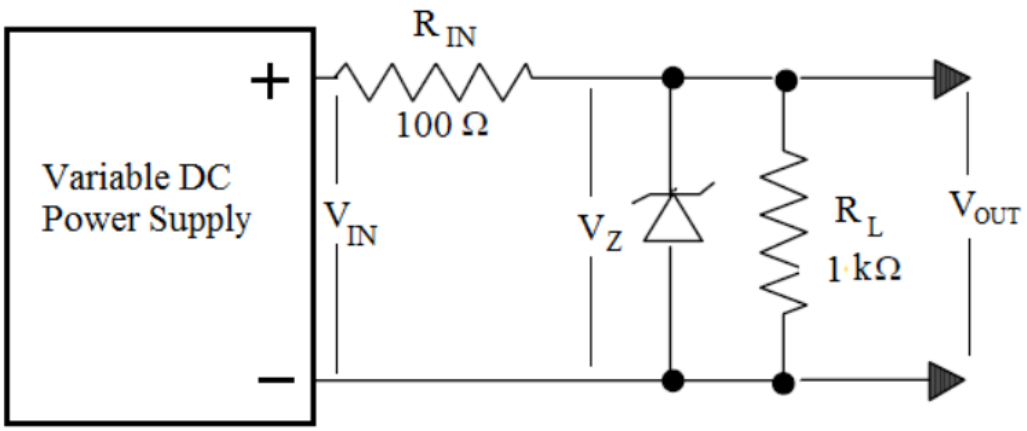

Fig 1. Electronic Circuit of Zener diode Voltage regulator

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Experimental Procedure:

A. I-V Characteristics of Zener Diode:

1. Identify the components required (power supply, voltmeter, ammeter, diode) and make the connections on bread board as per circuit diagram.
2. Connect the circuit diagram for diode in forward biasing mode.
3. Switch on the power supply and increase applied voltage gradually.
4. Note down the required readings.
5. Repeat steps 2 to 4 for reverse bias mode.
6. Tabulate the observations and plot the I-V curve for Zener diode in forward and reverse bias.
7. From your observations obtain the value of cut-in voltage and breakdown voltage V_Z.

B. Line regulation:

1. Identify the components required and make the connections on bread board as per circuit diagram.
2. Keep load resistance fixed value; vary DC input voltage from 0V to 15V and note down the value of output load voltage V_L.
3. Note down output load voltage with high line voltage V_{HL} and as a load voltage with low line voltage V_{LL}.
4. Plot the graphs for V_{IN} Vs V_L and calculate % line regulation.

C. Load regulation:

1. Identify the components required and make the connections on bread board as per circuit diagram.
2. Keep input voltage constant say 10V.
3. Vary R_L in steps of 1KΩ and note down the value of output load voltage V_L.
4. Note down no load voltage V_{NL} for maximum load resistance and full load voltage V_{FL} for minimum load resistance value.
5. Plot the graphs for R_L Vs V_L & calculate % load regulation.

Observation Table:

Table:1 (for Forward Bias Characteristics)

S. No.	Diode Voltage (volts)	Resistor Current (mA)	Diode Current (mA)
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			

Table:2 (for Reverse Bias Characteristics)

S. No.	Diode Voltage (volts)	Resistor Current (mA)	Diode Current (mA)
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			

Table:3 Line Regulation

Keep R_L = 1 KΩ, Vary supply voltage

S. No.	Supply Voltage, V_{IN} (volts)	Load Volatge, V_L (Volts)
1		
2		
3		
4		

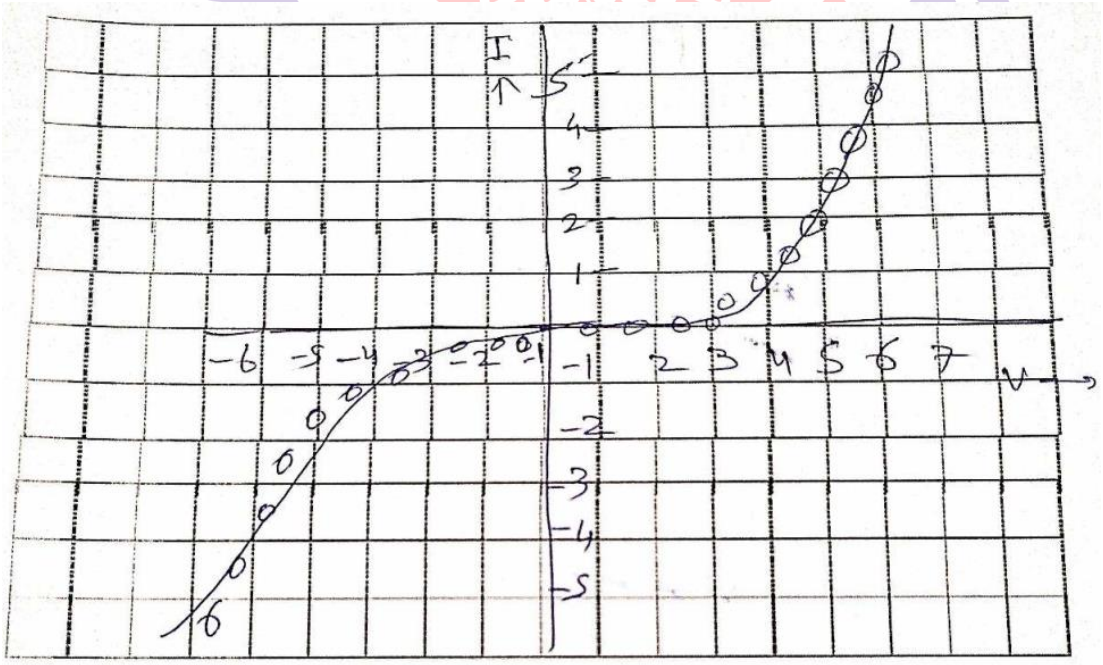
5		
6		
7		
8		
9		
10		

Table:4 Load Regulation

Keep V_{IN} = 10 V, Vary load resistor

S. No.	Load Resistor (KΩ)	Load Volatge, V_L (Volts)
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		

Model graph:



Calculation:

% Line regulation= $[(V_{HL}- V_{LL}) / V_{HL}]*100$ = _____%

% load regulation= $[(V_{NL}- V_{FL}) / V_{NL}]*100$ = _____%

Results:

Cut in voltage = _____ Volts

Breakdown voltage = _____ Volts

% Line regulation = _____%

% Load regulation = _____%

Precautions:

1. Connections should be done properly
2. Voltmeter and ammeter of appropriate ranges should be selected properly.
3. Turn off the setup box when it was used.
4. Never cross the limits specified by the manufacturer, otherwise the diode will get damaged.

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Experiment 3: Study of the I-V Characteristics of the Common Emitter Configuration of BJT and to obtain r_i, r_0 and β.

Objective: To study the I-V characteristics of the Common Emitter Configuration of BJT (NPN) and to obtain r_i, r_0, β.

Apparatus: a n-p-n transistor, Bread board, two batteries of 3 volts and 9 volts, a potentiometer of total resistance of the order of 1 MΩ and another of 25 K, a voltmeter of range 0-3 V, a voltmeter of 0-10 V, two ammeters of range 0-25 mA, connecting wires, etc.

Theory:

A Bipolar Junction Transistor, or BJT is a three terminal device having two PN junctions connected together in series. Each terminal is given a name to identify it and these are known as the Emitter (E), Base (B) and Collector (C). There are two basic types of bipolar transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. An NPN transistor has an N type emitter, a P type base and an N type collector while a PNP transistor has a P type emitter, an N type base and a P type collector. The emitter is heavily doped, base region is thin and lightly doped and collector is moderately doped and is the largest. The principle of operation of the two transistor types NPN and PNP, is exactly the

same the only difference being in the biasing (base current) and the polarity of the power supply for each type.

The current conduction in transistors takes place due to both charge carriers- that is electrons and holes and hence they are named Bipolar Junction Transistors (BJT). Bipolar Transistors are "CURRENT" Amplifying or current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing current applied to their base terminal. BJTs are extensively used in all types of electronic circuits. Two of the most important applications for the transistor are (1) as an amplifier in analog electronic systems, and (2) as a switch in digital systems.

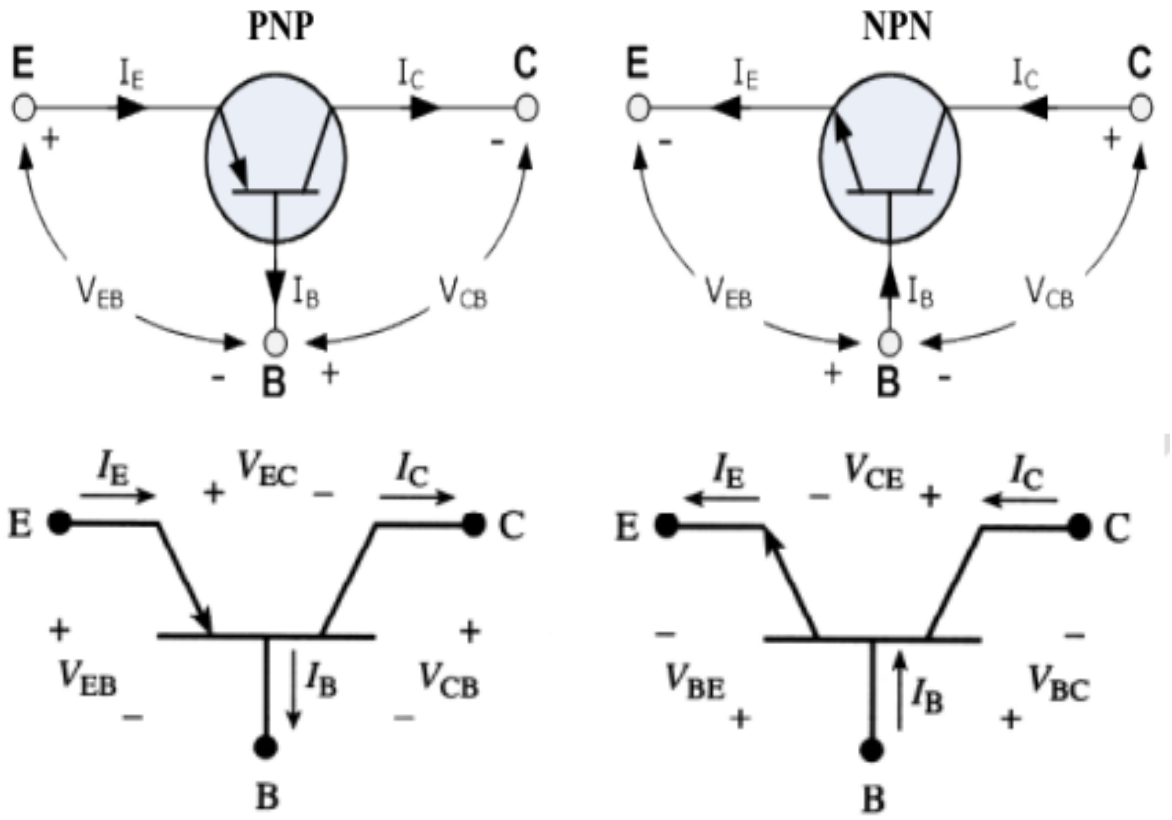


Fig 1. NPN and PNP configurations of a BJT Transistor.

The symbols for both the NPN and PNP bipolar transistor are shown above along with the direction of conventional current flow. The direction of the arrow in the symbol shows current flow between the base and emitter terminal,

pointing from the positive P-type region to the negative N-type region, exactly the same as for the standard diode symbol. For normal operation, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased.

The operation of the BJT is based on the principles of the PN junction as depicted in Fig. 2. In the NPN BJT, electrons are injected from the forward-biased emitter into the thin base region where, as minority carriers, they diffuse toward the reverse-biased collector. Some of these electrons recombine with holes in the base region, thus producing a small base current, I_B. The remaining electrons reach the collector where they provide the main source of carriers for the collector current, I_C. Thus, if there are no electrons injected from the emitter, there will be (almost) no collector current and, therefore, the emitter current controls the collector current. Combining currents, the total emitter current is given as $I_E = I_B + I_C$. For normal PNP operation, the polarity of both voltage sources must be reversed.

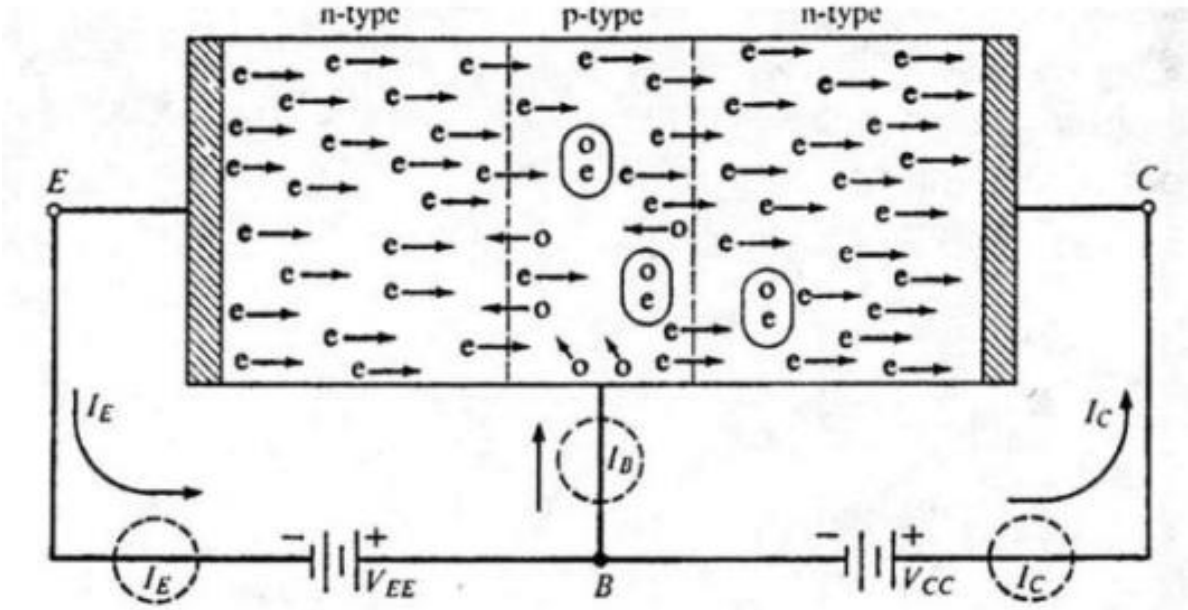


Fig. 2. Representation of NPN transistor in operation with forward biased emitter-base and reverse biased collector-base junction (e =electrons, O = holes, and Oe = recombination of holes and electrons)

BJTs are used to amplify current, using a small base current to control a large current between the collector and the emitter. This amplification is so important that one of the most noted parameters of gain, β (or h_{FE}), which is the ratio of collector current to base current.

Transistor Configurations:

Transistors when used as amplifiers, there is an input side to which an input signal is applied and an output side from which the output signal is taken. There are three possible configurations according to which electrode is common both to the input and to output signals when a transistor is connected in a circuit: (a) Common base, (b) Common emitter (c) Common collector. The common terminal is connected to the ground and accordingly the above three configurations are called grounded base, grounded emitter and grounded collector respectively.

We will be focusing on the common emitter configurations in this experiment. The behaviour of a transistor can be represented by d.c. current-voltage (I-V) curves, called the static characteristic curves of the device. The three important characteristics of a transistor are: (i) Input characteristics, (ii) Output characteristics and (iii) Transfer Characteristics. These characteristics give information about various transistor parameters, e.g. input and out dynamic resistance, current amplification factors, etc. When the BJT is used with the base and emitter terminals as the input and the collector and emitter terminals as the output, the current gain as well as the voltage gain is large. It is for this reason that this common-emitter (CE) configuration is the most useful connection for the BJT in electronic systems.

Operation regions and characteristics curves:

Depending upon the biasing of the two junctions, emitter-base (EB) junction and collector-base (CB) the transistor is said to be in one of the four modes of operation as described below:

Operating region	B-E Junction	B-C Junction	Features		
Cut-off	Reverse	Reverse	$I_B \approx I_C \approx I_E \approx 0$	Off state – no current (V_{BE}<0.7V)	
Saturation	Forward	Forward	Conducting structure	V_{BE}=0.7V	$V_{CE} \approx 0.2V$
Active	Forward	Reverse	Amplifier Gain: 100-1000	($I_C=\beta I_B$)	V_{BE}=0.7V V_{CE} >0.2V
Reverse-active	Reverse	Forward	Limited use Gain< 1	($I_B > I_C$)	

NOTE : V_{BE} will vary from 0.6 to 0.7 V

Common Emitter Transistor Characteristics:

In a common emitter configuration, emitter is common to both input and output as shown in its circuit diagram.

1. **Input Characteristics:** The variation of the Input current i.e. base current I_B with the base-emitter voltage V_{BE} keeping the collector-emitter voltage V_{CE} fixed, gives the input characteristic in CE mode.

   Input Dynamic Resistance (r_i): This is defined as the ratio of change in base emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). This is dynamic and it can be seen from the input characteristic, its value varies with the operating current in the transistor.

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}}$$

   The value of r_i can be anything from a few hundreds to a few thousand ohms.

   The input characteristic resembles a forward biased diode curve. After cut in voltage the I_B increases rapidly with small increase in V_{BE}. It means that dynamic input resistance is small in CE configuration.

2. **Output Characteristics:** The variation of the collector current I_C with the collector-emitter voltage, V_{CE} is called the output characteristic. The plot of I_C versus V_{CE} for different fixed values of I_B gives one output characteristic. Since the collector current changes with the base current, there will be different output characteristics corresponding to different values of I_B.

   The output characteristic of common emitter configuration consists of three regions: **Active, Saturation and Cut-off**

   Active region: In this region base-emitter junction is forward biased and base-collector junction is reversed biased. The curves are approximately horizontal in this region.

   Saturation region: In this region both the junctions are forward biased.

   Cut-off: In this region, both the junctions are reverse biased. When the base current is made equal to zero, the collector current is reverse leakage current I_{CEO}. The region below $I_B = 0$ is the called the cut-off region.

   Output Dynamic Resistance (r_o): This is defined as the ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at a constant base current I_B.

$$r_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B}$$

   The high magnitude of the output resistance (of the order of 100 kW) is due to the reverse-biased state of this diode.

3. **Transfer Characteristics:** The transfer characteristics are plotted between the input and output currents (I_B versus I_C). Both I_B and I_C increase proportionately.

   Current amplification factor (β): This is defined as the ratio of the change in collector current to the change in base current at a constant collector-emitter voltage (V_{CE}) when the transistor is in active state.

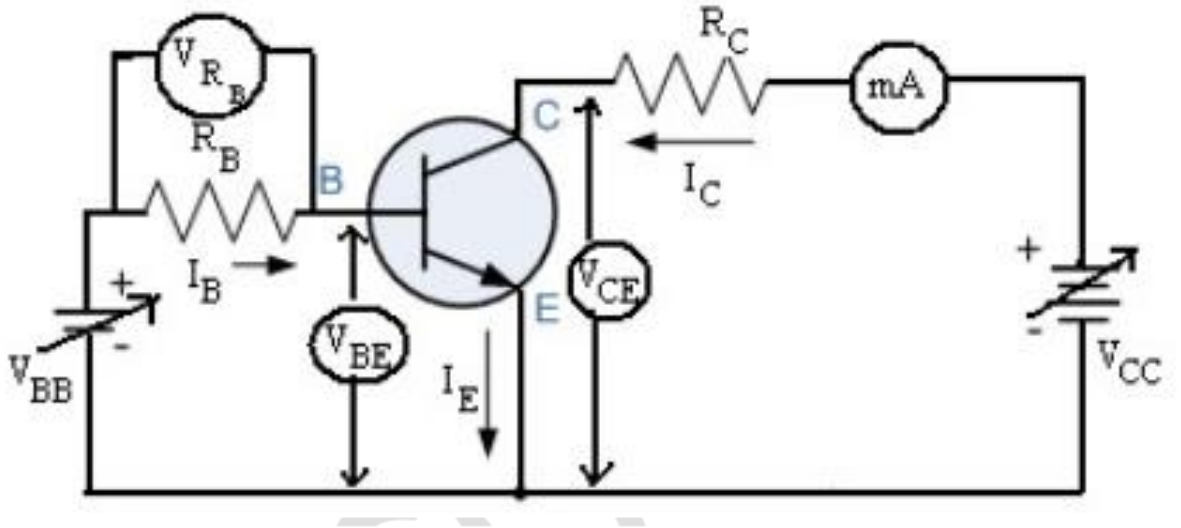
$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}}$$

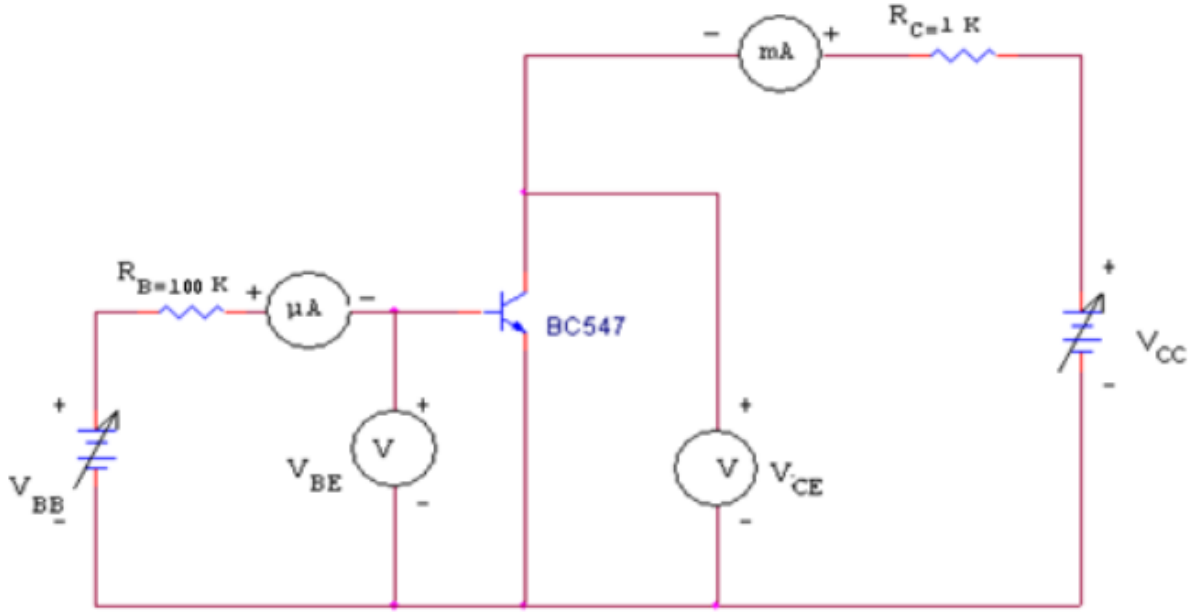
This is also known as small signal current gain and its value is very large. The ratio of I_C and I_B we get what is called βdc of the transistor. Hence,

$$\beta_{dc} = \left.\frac{I_C}{I_B}\right|_{V_{CE}}$$

Since IC increases with IB almost linearly, the values of both βdc and βac are nearly equal.

Test Circuit for NPN BJT input-output Characteristics in CE mode:





Experimental Procedure:

1. Note down the code of the transistor.
2. Identify different terminals (E, B and C) and the type (PNP/NPN) of the transistors.
3. Now configure CE circuit using the NPN transistor as per the circuit diagram. Use R_B = 100kΩ and R_C = 1 kΩ.
4. **For input characteristics,** first fix the voltage V_{CE} by adjusting V_{CC} to the minimum possible position. Now vary the voltage V_{BE} slowly (say, in steps of 0.05V) by varying V_{BB}. Measure V_{BE} using a multimeter. If V_{CE} varies during measurement bring it back to the set value. To determine I_B, measure V_{RB} across the resistor R_B and use the relation $I_B = V_{RB}/R_B$.
5. Repeat the above step for another value of V_{CE} say, 2V.
6. **For output characteristics**, first fix I_B = 0, i.e. V_{RB} = 0. By adjusting V_{CC}, vary the collector voltage V_{CE} in steps of say 1V and measure V_{CE} and the corresponding I_C using multimeters. If needed vary V_{CE} in negative direction as described for CB configuration and measure both V_{CE} and I_C, till you get 0 current.
7. Repeat the above step for at least 5 different values of I_B by adjusting V_{BB}. You may need to adjust V_{BB} continuously during measurement in order to maintain a constant I_B.
8. Plot the input and output characteristics by using the readings taken above and determine the input and output dynamic resistance.
9. **To plot transfer characteristics,** select a suitable voltage V_{CE} well within the active region of the output characteristics, which you have tabulated already (no need to take further data). Plot a graph between I_C and the corresponding I_B at the chosen voltage V_{CE}. Determine β_{ac} from the slope of this graph.

Observation Table:

Transistor code: _____, RB = _____, RC = _____.

Table:1 INPUT CHARACTERISTICS

S. No.	V_{CE} = V			V_{CE} = V		
	V_{BE} (V)	V_{RB} (V)	I_D (mA)	V_{BE} (V)	V_{RB} (V)	I_D (mA)
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						

Table:2 OUTPUT CHARACTERISTICS

S. No.	I_{B1} = 0 μA		I_{B2} = 30 μA		I_{B3} = 60 μA		I_{B4} = 90 μA		I_{B1} = 120 μA	
	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)
1										
2										
3										
4										
5										
6										
7										
8										
9										
10										

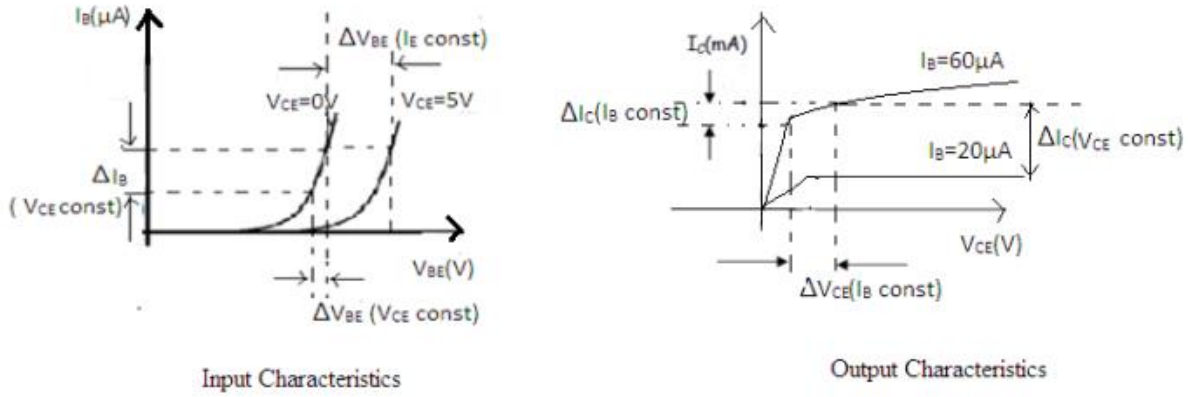
Table:3 TRANSFER CHARACTERISTICS

V_{CE} = ……. V

S. No.	I_B (μA)	I_C (mA)

1		
2		
3		
4		
5		

Model Plot:



Input Characteristics

Output Characteristics

Plotting graph and Calculation from graphs:

1. Plot the input characteristics by taking V_{BE} on X-axis and I_B on Y-axis keeping constant V_{CE} as a constant parameter.
2. Plot the output characteristics by taking V_{CE} on X-axis and taking I_C on Y-axis keeping I_B as a constant parameter.
3. Plot the transfer characteristics by taking I_B on X-axis and taking I_C on Y-axis keeping V_{CE} as a constant parameter.
4. To obtain input resistance find ΔV_{BE} and ΔI_B for a constant V_{CE} on one of the input characteristics. Input impedance = $h_{ie} = r_i = \Delta V_{BE} / \Delta I_B$ (V_{CE} is constant)
   Reverse voltage gain = $h_{re} = \Delta V_{EB}/\Delta V_{CE}$ (I_B = constant)
5. To obtain output resistance find ΔI_C and ΔV_{CB} at a constant I_B.
   Output admittance, $h_{oe} = 1/r_o = \Delta I_C / \Delta V_{CE}$ (I_B is constant)
   Forward small signal current gain = $h_{fe} = \Delta I_C / \Delta I_B$ (V_{CE} = constant)

Results:

The h-parameters for a transistor in CE configuration are:

a. The Input Resistance (h_{ie}) _____Ohms.

b. The Reverse Voltage Gain (h_{re}) _____.

c. The Output Conductance (h_{oe}) _____ Mhos.

d. The Forward Current Gain (h_{fe}) _____.

Precautions:

1. Connections should be done properly.
2. Voltmeter and ammeter of appropriate ranges should be selected properly.
3. Turn off the setup circuit when it was used.
4. Never cross the limits specified by the manufacturer, otherwise the diode will get damaged.

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Department of Pure & Applied Physics

Condensed Matter Physics Practical Experiment Manual

Experiment 4: Study of the I-V Characteristics of the Common Base Configuration of BJT and to obtain r_i, r_0 and α.

Objective: To study the I-V characteristics of the Common Base Configuration of BJT (NPN) and to obtain r_i, r_0, α.

Apparatus: a n-p-n transistor, Bread board, two batteries of 3 volts and 9 volts, a potentiometer of total resistance of the order of 1 MΩ and another of 25 K, a voltmeter of range 0-3 V, a voltmeter of 0-10 V, two ammeters of range 0-25 mA, connecting wires, etc.

Theory:

A Bipolar Junction Transistor, or BJT is a three terminal device having two PN junctions connected together in series. Each terminal is given a name to identify it and these are known as the Emitter (E), Base (B) and Collector (C). There are two basic types of bipolar transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. An NPN transistor has an N type emitter, a P type base and an N type collector while a PNP transistor has a P type emitter, an N type base and a P type collector. The emitter is heavily doped, base region is thin and lightly doped and collector is moderately doped and is the largest. The principle of operation of the two transistor types NPN and PNP, is exactly the

same the only difference being in the biasing (base current) and the polarity of the power supply for each type.

The current conduction in transistors takes place due to both charge carriers- that is electrons and holes and hence they are named Bipolar Junction Transistors (BJT). Bipolar Transistors are "CURRENT" Amplifying or current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing current applied to their base terminal. BJTs are extensively used in all types of electronic circuits. Two of the most important applications for the transistor are (1) as an amplifier in analog electronic systems, and (2) as a switch in digital systems.

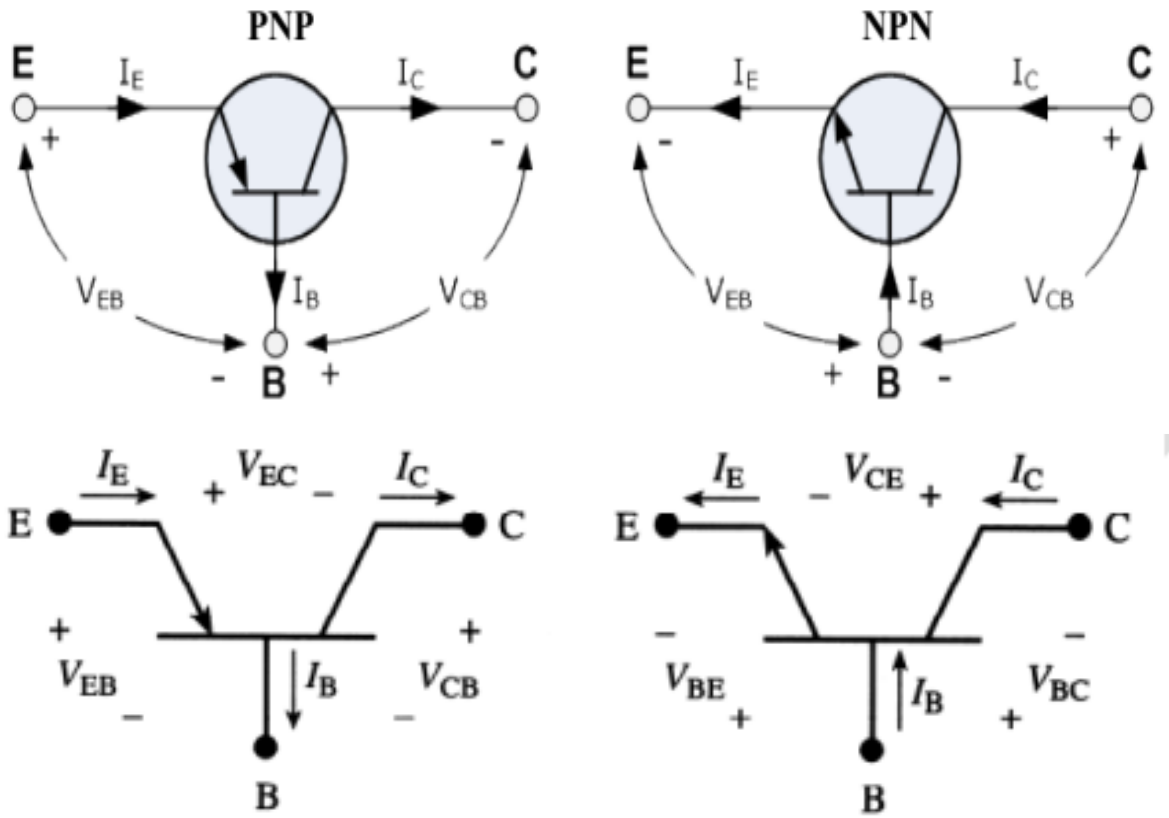


Fig 1. NPN and PNP configurations of a BJT Transistor.

The symbols for both the NPN and PNP bipolar transistor are shown above along with the direction of conventional current flow. The direction of the arrow

in the symbol shows current flow between the base and emitter terminal, pointing from the positive P-type region to the negative N-type region, exactly the same as for the standard diode symbol. For normal operation, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased.

The operation of the BJT is based on the principles of the PN junction as depicted in Fig. 2. In the NPN BJT, electrons are injected from the forward-biased emitter into the thin base region where, as minority carriers, they diffuse toward the reverse-biased collector. Some of these electrons recombine with holes in the base region, thus producing a small base current, I_B. The remaining electrons reach the collector where they provide the main source of carriers for the collector current, I_C. Thus, if there are no electrons injected from the emitter, there will be (almost) no collector current and, therefore, the emitter current controls the collector current. Combining currents, the total emitter current is given as $I_E = I_B + I_C$. For normal PNP operation, the polarity of both voltage sources must be reversed.

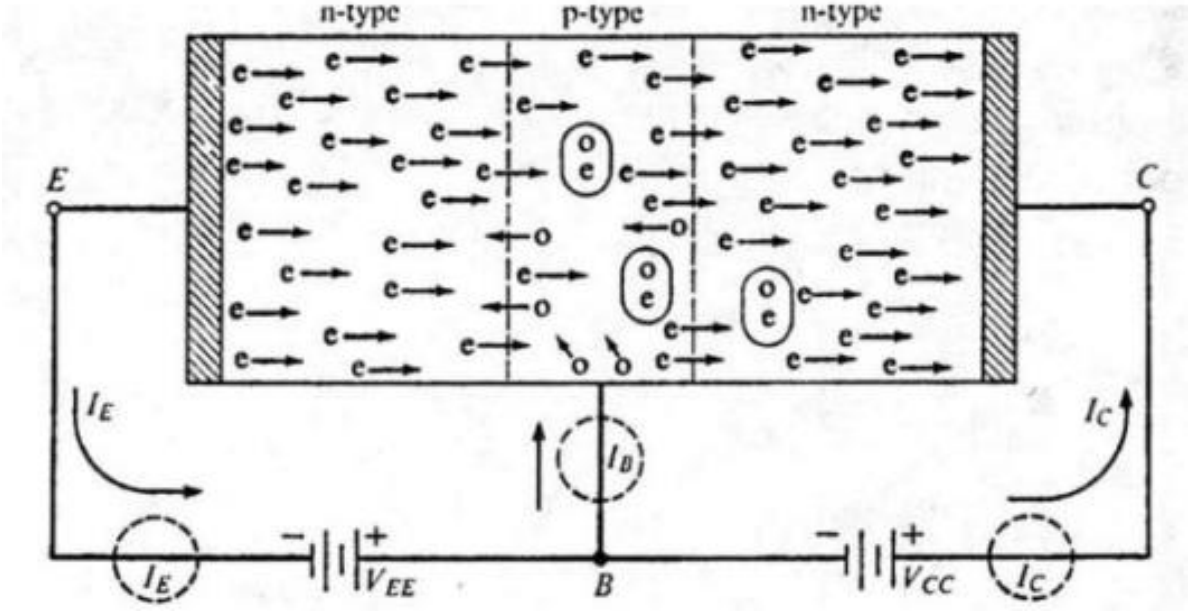


Fig. 2. Representation of NPN transistor in operation with forward biased emitter-base and reverse biased collector-base junction (e =electrons, O = holes, and Oe = recombination of holes and electrons)

BJTs are used to amplify current, using a small base current to control a large current between the collector and the emitter. This amplification is so important that one of the most noted parameters of gain, β (or h_{FE}), which is the ratio of collector current to base current.

Transistor Configurations:

Transistors when used as amplifiers, there is an input side to which an input signal is applied and an output side from which the output signal is taken. There are three possible configurations according to which electrode is common both to the input and to output signals when a transistor is connected in a circuit: (a) Common base, (b) Common emitter (c) Common collector. The common terminal is connected to the ground and accordingly the above three configurations are called grounded base, grounded emitter and grounded collector respectively.

We will be focusing on the common base configurations in this experiment.

The behaviour of a transistor can be represented by d.c. current-voltage (I-V) curves, called the static characteristic curves of the device. The three important characteristics of a transistor are: (i) Input characteristics, (ii) Output characteristics and (iii) Transfer Characteristics. These characteristics give information about various transistor parameters, e.g. input and out dynamic resistance, current amplification factors, etc. In common base configuration, emitter is the input terminal, collector is the output terminal and base terminal is connected as a common terminal for both input and output. That means the emitter terminal and common base terminal are known as input terminals whereas the collector terminal and common base terminal are known as output terminals.

In common base configuration, the base terminal is grounded so the common base configuration is also known as grounded base configuration. Sometimes common base configuration is referred to as common base amplifier, CB amplifier, or CB configuration. The input signal is applied between the emitter and base terminals while the corresponding output signal is taken across the collector and base terminals. Thus, the base terminal of a transistor is common for both input and output terminals and hence it is named as common base configuration. The supply voltage between base and emitter is denoted by V_{BE} while the supply voltage between collector and base is denoted by V_{CB}. In every configuration, the base-emitter junction is always forward biased and collector-base junction is always reverse biased. Therefore, in common base configuration, the base-emitter junction JE is forward biased and collector-base junction is reverse biased.

Common Base Transistor Characteristics:

In a common base configuration, base is common to both input and output as shown in its circuit diagram.

1. **Input Characteristics:** The variation of the Input current i.e. emitter current I_E with the base-emitter voltage V_{BE} keeping the collector-base voltage V_{CB} fixed, gives the input characteristic in CB mode. First, draw a vertical line and horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The input current or emitter current (IE) is taken along the y-axis (vertical line) and the input voltage (V_{BE}) is taken along the x-axis (horizontal line).

   To determine the input characteristics, the output voltage V_{CB} (collector-base voltage) is kept constant at zero volts and the input voltage V_{BE} is increased from zero volts to different voltage levels. For each voltage level of the input voltage (V_{BE}), the input current (I_E) is recorded on a paper or in any other form. A curve is then drawn between input current I_E and input voltage V_{BE} at

constant output voltage V_{CB} (0 volts). The output voltage (V_{CB}) is increased from zero volts to a certain voltage level (8 volts) and kept constant at 8 volts. While increasing the output voltage (V_{CB}), the input voltage (V_{BE}) is kept constant at zero volts. After kept the output voltage (V_{CB}) constant at 8 volts, the input voltage V_{BE} is increased from zero volts to different voltage levels. For each voltage level of the input voltage (V_{BE}), the input current (I_E) is recorded on a paper or in any other form. A curve is then drawn between input current I_E and input voltage V_{BE} at constant output voltage V_{CB} (8 volts). This is repeated for higher fixed values of the output voltage (V_{CB}). When output voltage (V_{CB}) is at zero volts and emitter-base junction is forward biased by the input voltage (V_{BE}), the emitter-base junction acts like a normal p-n junction diode. So, the input characteristics are same as the forward characteristics of a normal pn junction diode. The cut in voltage of a silicon transistor is 0.7 volts and germanium transistor is 0.3 volts. A small increase in input voltage (V_{BE}) will rapidly increase the input current (I_E). When the output voltage (V_{CB}) is increased from zero volts to a certain voltage level (8 volts), the emitter current flow will be increased which in turn reduces the depletion region width at emitter-base junction. As a result, the cut in voltage will be reduced. Therefore, the curves shifted towards the left side for higher values of output voltage V_{CB}.

Input Dynamic Resistance (r_i): This is defined as the ratio of change in base emitter voltage (ΔV_{BE}) to the resulting change in emitter current (ΔI_E) at constant collector-base voltage (V_{CB}). This is dynamic and it can be seen from the input characteristic, its value varies with the operating current in the transistor.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_E}, \qquad V_{CB} = \text{constant}$$

The value of r_i of a common base amplifier is very low.

2. **Output Characteristics:** The output characteristics describe the relationship between output current (I_C) and the output voltage (V_{CB}). First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The output current or collector current (I_C) is taken along the y-axis (vertical line) and the output voltage (V_{CB}) is taken along the x-axis (horizontal line). To determine the output characteristics, the input current or emitter current I_E is kept constant at zero mA and the output voltage V_{CB} is increased from zero volts to different voltage levels. For each voltage level of the output voltage V_{CB}, the output current (I_C) is recorded. A curve is then drawn between output current I_C and output voltage V_{CB} at constant input current I_E (0 mA). When the emitter current or input current I_E is equal to 0 mA, the transistor operates in the cut-off region. Next, the input current (I_E) is increased from 0 mA to 1 mA by adjusting the input voltage V_{BE} and the input current I_E is kept constant at 1 mA. While increasing the input current I_E, the output voltage V_{CB} is kept constant. After kept the input current (I_E) constant at 1 mA, the output voltage (V_{CB}) is increased from zero volts to different voltage levels. For each voltage level of the output voltage (V_{CB}), the output current (I_C) is recorded. A curve is then drawn between output current I_C and output voltage V_{CB} at constant input current I_E (1 mA). This region is known as the active region of a transistor. This is repeated for higher fixed values of input current IE (I.e. 2 mA, 3 mA, 4 mA and so on). From the above characteristics, can see that for a constant input current I_E, when the output voltage V_{CB} is increased, the output current I_C remains constant. At saturation region, both emitter-base junction and collector-base junction are forward biased. Here, we can see that a sudden increase in the collector current when the output voltage V_{CB} makes the collector-base junction forward biased.

Output Dynamic Resistance (r_o): This is defined as the ratio of change in output voltage i.e. collector-emitter voltage (ΔV_{CB}) to the change in collector current (ΔI_C) at a constant emitter current I_E.

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C}, \qquad I_E = \text{constant}$$

The output resistance of common base amplifier is very high.

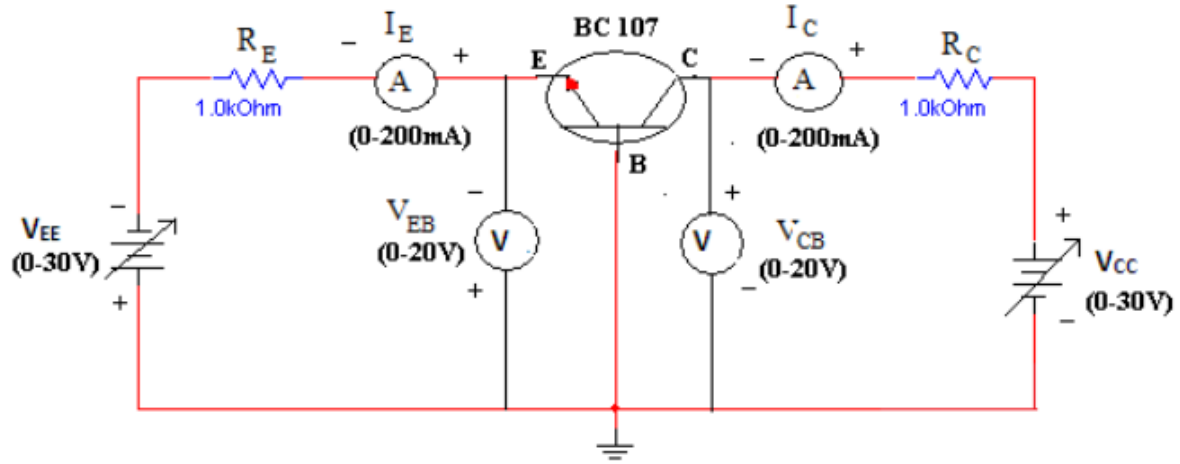
Transfer Characteristics: The transfer characteristics are plotted between the input and output currents (I_E versus I_C). Both I_E and I_C increase proportionately.

Current gain (α): This is defined as the ratio of output collector current, I_B to the input emitter current I_E, at a constant collector-emitter voltage (V_{CB}) when the transistor is in active state.

$$\alpha = \frac{I_C}{I_E}$$

The current gain of a transistor in CB configuration is less than unity. The typical current gain of a common base amplifier is 0.98.

Test Circuit for NPN BJT input-output Characteristics in CE mode:



Experimental Procedure:

1. Note down the code of the transistor.

2. Identify different terminals (E, B and C) and the type (PNP/NPN) of the transistors.
3. Now configure CE circuit using the NPN transistor as per the circuit diagram. Use R_B = 100kΩ and R_C = 1 kΩ.
4. **For input characteristics,**

   Keep output voltage V_{CB} = 0V by varying V_{CC}. Then varying V_{EE} gradually, note down emitter current I_E and emitter-base voltage (V_{EE}). Step size is not fixed because of nonlinear curve. Initially vary V_{EE} in steps of 0.1 V. Once the current starts increasing vary V_{EE} in steps of 1V up to 12V. Repeat above procedure for V_{CB} = 4V.

5. **For output characteristics**

   Keep emitter current I_E = 5mA by varying V_{EE}. Varying V_{CC} gradually in steps of 1V up to 12V and note down collector current I_C and collector-base voltage (V_{CB}). Then Repeat above procedure for I_E = 10mA. 5. Repeat above procedure (step 3) for IE = 10mA.Plot the input and output characteristics by using the readings taken above and determine the input and output dynamic resistance.
5. **To plot transfer characteristics,** select a suitable voltage V_{CE} well within the active region of the output characteristics, which you have tabulated already (no need to take further data). Plot a graph between I_C and the corresponding I_B at the chosen voltage V_{CE}. Determine β_{ac} from the slope of this graph.

Observation Table:

Transistor code: _____, RB = _____, RC = _____.

Table:1 INPUT CHARACTERISTICS

S. No.	V_{CB} = 0 V			V_{CB} = 4 V		
	V_{EB} (V)	V_{EE} (V)	I_E (mA)	V_{EB} (V)	V_{EE} (V)	I_E (mA)
1						

2						
3						
4						
5						
6						
7						
8						
9						
10						

Table:2 OUTPUT CHARACTERISTICS

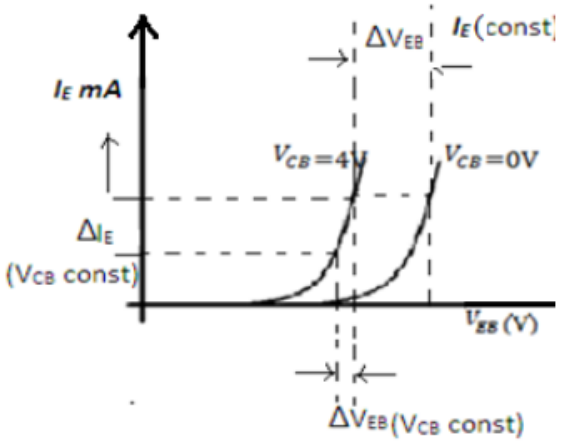
S. NO.	V_{CC} (V)	I_{E1} = 0 mA		I_{E2} = 3 mA		I_{E3} = 6 mA		I_{E4} = 9 mA		I_{E5} = 12 mA	
		V_{CE} (V)	I_C (mA)	V_{CB} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)
1											
2											
3											
4											
5											
6											
7											
8											
9											
10											

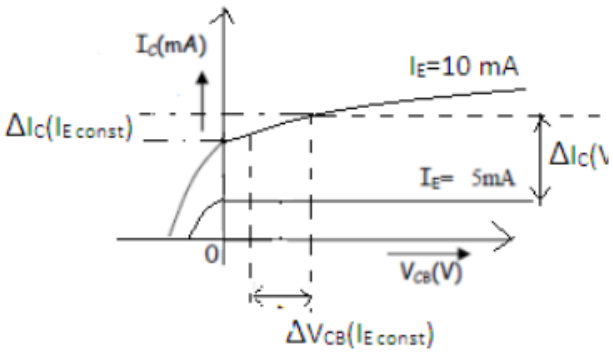
Table:3 TRANSFER CHARACTERISTICS

V_{CB} = ……. V

S. No.	I_E (mA)	I_C (mA)
1		
2		
3		
4		
5		

Model Plot:





Plotting graph and Calculation from graphs:

1. Plot the input characteristics for different values of V_{CB} by taking V_{EE} on X-axis and taking I_E on Y-axis keeping V_{CB} as a constant parameter.
2. Plot the output characteristics by taking V_{CB} on X-axis and taking I_C on Y-axis keeping I_E as a constant parameter.
3. Plot the transfer characteristics by taking I_E on X-axis and taking I_C on Y-axis keeping V_{CB} as a constant parameter.
4. To obtain input resistance find ΔV_{EE} and ΔI_E for a constant V_{CB} on one of the input characteristics. Input impedance = $h_{ib} = r_i = \Delta V_{EE} / \Delta I_E$ (V_{CB} is constant)
   Reverse voltage gain = $h_{rb} = \Delta V_{EB}/\Delta V_{CB}$ (I_E = constant)
5. To obtain output resistance find ΔI_C and ΔV_{CB} at a constant I_E.
   Output admittance, $h_{ob} = 1/r_o = \Delta I_C / \Delta V_{CB}$ (I_E is constant)
   Forward small signal current gain = $h_{fb} = \Delta I_C / \Delta I_E$ (V_{CB} = constant)

Results:

The h-parameters for a transistor in CB configuration are:

a. The Input Resistance (h_{ib}) _____Ohms.

b. The Reverse Voltage Gain (h_{rb}) _____.

c. The Output Admittance (h_{ob}) _____ Mhos.

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d. The Forward Current Gain (h_{fb}) _____.

Precautions:

1. Connections should be done properly.
2. Voltmeter and ammeter of appropriate ranges should be selected properly.
3. Turn off the setup circuit when it was used.
4. Never cross the limits specified by the manufacturer, otherwise the diode will get damaged.

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Department of Pure & Applied Physics

Condensed Matter Physics Practical Experiment Manual

Experiment 5: Study of the I-V Characteristics of the Common Collector Configuration of BJT and to obtain Voltage gain, r_i and r_0

Objective: To study the I-V characteristics of the Common Collector Configuration of BJT (NPN) and to obtain voltage gain, r_i and r_0.

Apparatus: a n-p-n transistor, Bread board, two batteries of 3 volts and 9 volts, a potentiometer of total resistance of the order of 1 MΩ and another of 25 K, a voltmeter of range 0-3 V, a voltmeter of 0-10 V, two ammeters of range 0-25 mA, connecting wires, etc.

Theory:

A Bipolar Junction Transistor, or BJT is a three terminal device having two PN junctions connected together in series. Each terminal is given a name to identify it and these are known as the Emitter (E), Base (B) and Collector (C). There are two basic types of bipolar transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. An NPN transistor has an N type emitter, a P type base and an N type collector while a PNP transistor has a P type emitter, an N type base and a P type collector. The emitter is heavily doped, base region is thin and lightly doped and collector is moderately doped and is the largest. The principle of operation of the two transistor types NPN and PNP, is exactly the

same the only difference being in the biasing (base current) and the polarity of the power supply for each type.

The current conduction in transistors takes place due to both charge carriers- that is electrons and holes and hence they are named Bipolar Junction Transistors (BJT). Bipolar Transistors are "CURRENT" Amplifying or current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing current applied to their base terminal. BJTs are extensively used in all types of electronic circuits. Two of the most important applications for the transistor are (1) as an amplifier in analog electronic systems, and (2) as a switch in digital systems.

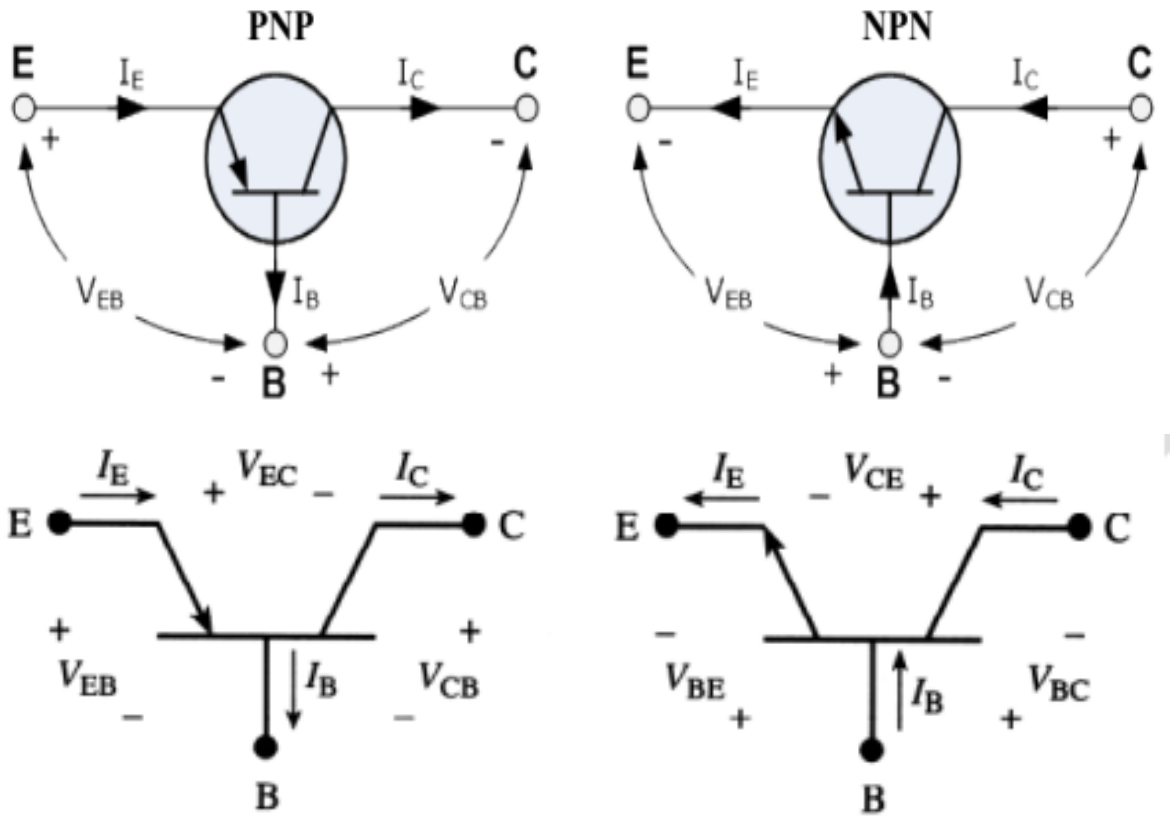


Fig 1. NPN and PNP configurations of a BJT Transistor.

The symbols for both the NPN and PNP bipolar transistor are shown above along with the direction of conventional current flow. The direction of the arrow

in the symbol shows current flow between the base and emitter terminal, pointing from the positive P-type region to the negative N-type region, exactly the same as for the standard diode symbol. For normal operation, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased.

The operation of the BJT is based on the principles of the PN junction as depicted in Fig. 2. In the NPN BJT, electrons are injected from the forward-biased emitter into the thin base region where, as minority carriers, they diffuse toward the reverse-biased collector. Some of these electrons recombine with holes in the base region, thus producing a small base current, I_B. The remaining electrons reach the collector where they provide the main source of carriers for the collector current, I_C. Thus, if there are no electrons injected from the emitter, there will be (almost) no collector current and, therefore, the emitter current controls the collector current. Combining currents, the total emitter current is given as $I_E = I_B + I_C$. For normal PNP operation, the polarity of both voltage sources must be reversed.

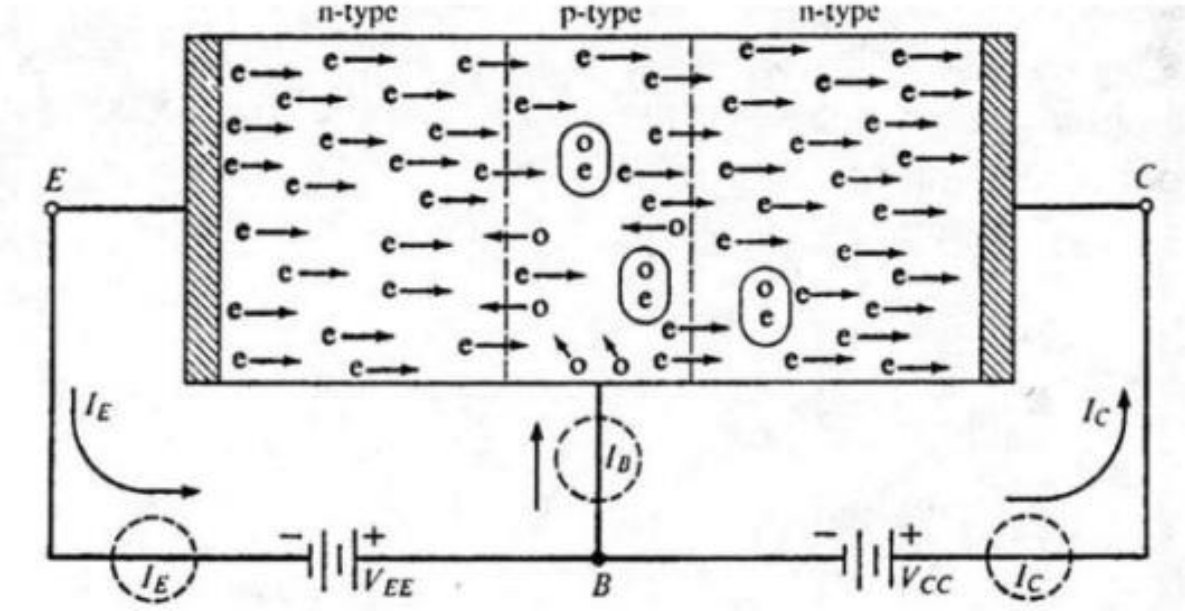


Fig. 2. Representation of NPN transistor in operation with forward biased emitter-base and reverse biased collector-base junction (e =electrons, O = holes, and Oe = recombination of holes and electrons)

BJTs are used to amplify current, using a small base current to control a large current between the collector and the emitter. This amplification is so important that one of the most noted parameters of gain, β (or h_{FE}), which is the ratio of collector current to base current.

Transistor Configurations:

Transistors when used as amplifiers, there is an input side to which an input signal is applied and an output side from which the output signal is taken. There are three possible configurations according to which electrode is common both to the input and to output signals when a transistor is connected in a circuit: (a) Common base, (b) Common emitter (c) Common collector. The common terminal is connected to the ground and accordingly the above three configurations are called grounded base, grounded emitter and grounded collector respectively.

We will be focusing on the common collector configurations in this experiment. The behaviour of a transistor can be represented by d.c. current-voltage (I-V) curves, called the static characteristic curves of the device. The three important characteristics of a transistor are: (i) Input characteristics, (ii) Output characteristics and (iii) Transfer Characteristics. These characteristics give information about various transistor parameters, e.g. input and out dynamic resistance, current amplification factors, etc. In this configuration we use collector terminal as common for both input and output signals. This configuration is also known as emitter follower configuration because the emitter voltage follows the base voltage. This configuration is mostly used as a buffer. These configurations are widely used in impedance matching applications

because of their high input impedance. In this configuration the input signal is applied between the base-collector region and the output is taken from the emitter-collector region. Here the input parameters are V_{BC} and I_B and the output parameters are V_{EC} and I_E. The common collector configuration has high input impedance and low output impedance. The input and output signals are in phase. Here also the emitter current is equal to the sum of collector current and the base current. This common collector configuration is a non-inverting amplifier circuit. The voltage gain for this circuit is less than unity but it has large current gain because the load resistor in this circuit receives both the collector and base currents.

Common Collector Transistor Characteristics:

In a common collector configuration, collector is common to both input and output as shown in its circuit diagram.

1. **Input Characteristics:** The variation of the Input current i.e. base current I_B with the input voltage or base-collector voltage V_{BC} keeping the emitter-collector-voltage V_{EC} fixed, gives the input characteristic in CC mode. First, draw a vertical line and horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The input current or base current (I_B) is taken along the y-axis (vertical line) and the input voltage or base-collector (V_{BC}) is taken along the x-axis (horizontal line).

   To determine the input characteristics, the output voltage V_{EC} is kept constant at 3V and the input voltage V_{BC} is increased from zero volts to different voltage levels. For each level of input voltage V_{BC}, the corresponding input current I_B is noted. A curve is then drawn between input current IB and input voltage V_{BC} at constant output voltage V_{EC} (3V). Next, the output voltage V_{EC} is increased from 3V to different voltage level, say for example 5V and then kept constant at 5V. While increasing the output voltage V_{EC}, the input voltage

V_{BC} is kept constant at zero volts. After kept the output voltage V_{EC} constant at 5V, the input voltage V_{BC} is increased from zero volts to different voltage levels. For each level of input voltage V_{BC}, the corresponding input current I_B is noted. A curve is then drawn between input current I_B and input voltage V_{BC} at constant output voltage V_{EC} (5V). This process is repeated for higher fixed values of output voltage (V_{EC}).

Input Dynamic Resistance (r_i): This is defined as the ratio of change in input base-collector voltage (ΔV_{BC}) to the resulting change in base current (ΔI_B) at constant emitter-collector- voltage (V_{EC}). This is dynamic and it can be seen from the input characteristic, its value varies with the operating current in the transistor.

$$r_i = \frac{\Delta V_{BC}}{\Delta I_B}, \qquad V_{EC} = \text{constant}$$

The value of r_i of a common collector amplifier is high.

2. **<u>Output Characteristics:</u>** The output characteristics describe the relationship between output current or emitter current (I_E) and output voltage or emitter-collector voltage (V_{EC}). The output current or emitter current (I_E) is taken along y-axis (vertical line) and the output voltage or emitter-collector voltage (V_{EC}) is taken along x-axis (horizontal line). To determine the output characteristics, the input current I_B is kept constant at zero micro amperes and the output voltage V_{EC} is increased from zero volts to different voltage levels. For each level of output voltage V_{EC}, the corresponding output current I_E is noted. A curve is then drawn between output current I_E and output voltage V_{EC} at constant input current I_B (0 μA). Next, the input current (I_B) is increased from 0 μA to 20 μA and then kept constant at 20 μA. While increasing the input current (I_B), the output voltage (V_{EC}) is kept constant at 0 volts. After kept the input current (I_B) constant at 20 μA, the output voltage (V_{EC}) is increased from zero volts to different voltage levels. For each level of output

voltage (V_{EC}), the corresponding output current (I_E) is recorded. A curve is then drawn between output current I_E and output voltage V_{EC} at constant input current I_B (20μA). This region is known as the active region of a transistor. This process is repeated for higher fixed values of input current I_B (I.e. 40 μA, 60 μA, 80 μA and so on).

In common collector configuration, if the input current or base current is zero then the output current or emitter current is also zero. As a result, no current flows through the transistor. So, the transistor will be in the cut-off region. If the base current is slightly increased, then the output current or emitter current also increases. So, the transistor falls into the active region. If the base current is heavily increased, then the current flowing through the transistor also heavily increases. As a result, the transistor falls into the saturation region.

Output Dynamic Resistance (r_o): This is defined as the ratio of change in output voltage i.e. emitter-collector voltage (ΔV_{EC}) to the change in output emitter current (ΔI_E) at a constant base current I_B.

$$r_o = \frac{\Delta V_{EC}}{\Delta I_E}, \quad I_B = \text{constant}$$

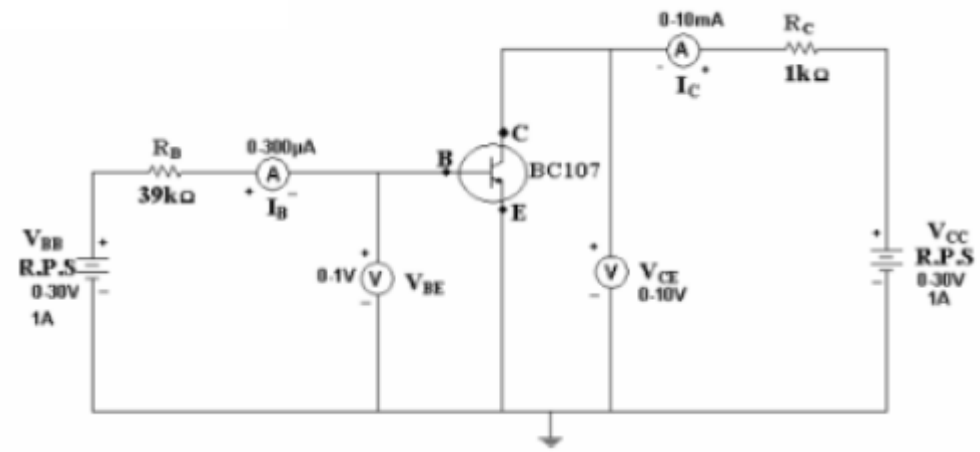
The output resistance of common base amplifier is low.

Current amplification factor (γ): This is defined as the ratio of change in output emitter current, I_E to the input base current I_B.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

The current gain of a transistor in CC configuration is high.

Test Circuit for NPN BJT input-output Characteristics in CE mode:



Experimental Procedure:

1. Note down the code of the transistor.
2. Identify different terminals (E, B and C) and the type (PNP/NPN) of the transistors.
3. Now configure CE circuit using the NPN transistor as per the circuit diagram. Use R_B = 100kΩ and R_C = 1 kΩ.
4. **For input characteristics,**

   Keep output voltage V_{CE} = 2V by varying V_{CC}. Then varying V_{BB} gradually, note down base current I_B and emitter-base voltage (V_{EE}). Step size is not fixed because of nonlinear curve. Initially vary V_{EE} in steps of 0.1 V. Once the current starts increasing vary V_{EE} in steps of 1V up to 12V. Repeat above procedure for V_{CE} = 5V and 10V

5. **For output characteristics**

   Keep base current constant at I_B = 10μA (say). Varying output voltage V_{CC} gradually in steps. Note down collector current I_C and collector-emitter voltage (V_{CE}). Then Repeat above procedure for I_E = 20 μA, 30μA, 40μA etc. Plot the input and output characteristics by using the readings taken above and determine the input and output dynamic resistance.

Observation Table:

Study of the I-V Characteristics of the Common Collector Configuration of BJT and to obtain voltage gain, ri and r0

Transistor code: _____, RB = _____, RC = _____.

Table:1 INPUT CHARACTERISTICS

S. No.	Applied voltage, V_{BB} (V)	V_{CB} = 2 V		V_{CB} = 5 V		V_{CB} = 5 V	
		V_{BE} (V)	I_B (μA)	V_{BE} (V)	I_B (μA)	V_{BE} (V)	I_B (μA)
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							

Table:2 OUTPUT CHARACTERISTICS

S. NO.	V_{CC} (V)	I_{B1} = 10 μA		I_{B2} = 30 μA		I_{B3} = 50 μA		I_{B4} = 70 μA		I_{B5} = 90 μA	
		V_{CE} (V)	I_C (mA)	V_{CB} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)
1											
2											
3											
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5											
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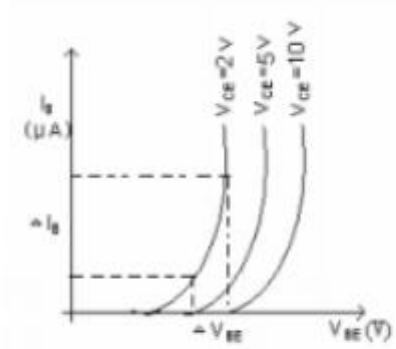
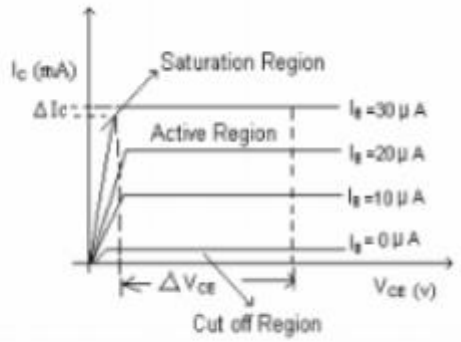
8											
9											
10											

Model Plot:



Input Characteristics



Output Characteristics

Plotting graph and Calculation from graphs:

1. Plot the input characteristics for different values of V_{CE} by taking V_{BE} on X-axis and taking I_B on Y-axis keeping V_{CC} as a constant parameter.
2. Plot the output characteristics by taking V_{CE} on X-axis and taking I_C on Y-axis keeping I_B as a constant parameter.
3. Plot the transfer characteristics by taking I_E on X-axis and taking I_C on Y-axis keeping V_{CB} as a constant parameter.
4. To obtain input resistance find ΔV_{BC} and ΔI_B for a constant V_{CB} on one of the input characteristics. Input impedance = $h_{ic} = r_i = \Delta V_{BC} / \Delta I_B$ (V_{EC} is constant)
5. To obtain output resistance find ΔI_E and ΔV_{EC} at a constant B_E.
   Output admittance, $h_{ob} = 1/r_o = \Delta I_E / \Delta V_{EC}$ (I_B is constant)
   Forward small signal current gain = $h_{fc} = \Delta I_E / \Delta I_B$

Results:

The h-parameters for a transistor in CC configuration are:

a. The Input Resistance (h_{ic}) _____Ohms.

b. The Output Admittance (h_{oc}) _____ Mhos.

c. The Forward Current Gain (h_{fc}) _____.

Precautions:

1. Connections should be done properly.
2. Voltmeter and ammeter of appropriate ranges should be selected properly.
3. Turn off the setup circuit when it was used.
4. Never cross the limits specified by the manufacturer, otherwise the diode will get damaged.

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Condensed Matter Physics Practical Experiment Manual

Experiment 6: Study of the I-V Characteristics of UJT

Objective:

To observe the I-V characteristics of Uni-junction transistor (UJT) and to calculate the Intrinsic Stand-Off Ratio (η)

Apparatus: UJT Characteristics apparatus comprised of:

1. Two continuously variable DC regulated power supplies of 0-15V for Emitter and 0-25V for B2 & B1 provided.
2. Three meters (or multimeters) to measure voltage & current which are mounted on front panel & connections brought out on sockets.
3. One UJT No. 2N2646 soldered behind the front panel & connections are brought out on sockets.

Theory:

A Uni-Junction Transistor (UJT) as the name implies, is characterized by a single P-N junction and a three terminal semiconductor switching device. This devise has the unique characteristic that when it is triggered, the Emitter current increases regeneratively until it is limited by Emitter power supply. It exhibits negative resistance characteristic that makes it useful in oscillator circuits as a switching device for pulse generator, saw tooth generator etc. The symbol for UJT is shown in Fig. 1a. The UJT is having three terminals base1 (B1), base2 (B2) and emitter (E). The UJT is made up of a very lightly doped N-type silicon bar with an electrical connection on each end and it acts as the base as shown in

Fig. 1b. In original UJT, a P-type impurity is heavily diffused into the base somewhere along its length near to B2 than B1, producing a single PN junction between the P type Emitter and bar. The lead to this junction is called the emitter lead E. With one PN junction, this device exhibits the properties of a conventional diode. Because the base terminals are taken from one section of the diode, this device is also called double based diode. The Emitter is heavily doped with many holes and the n-region is lightly doped and thus the resistance between the base terminals is very high (5 kΩ to 10 kΩ) when Emitter lead is open.

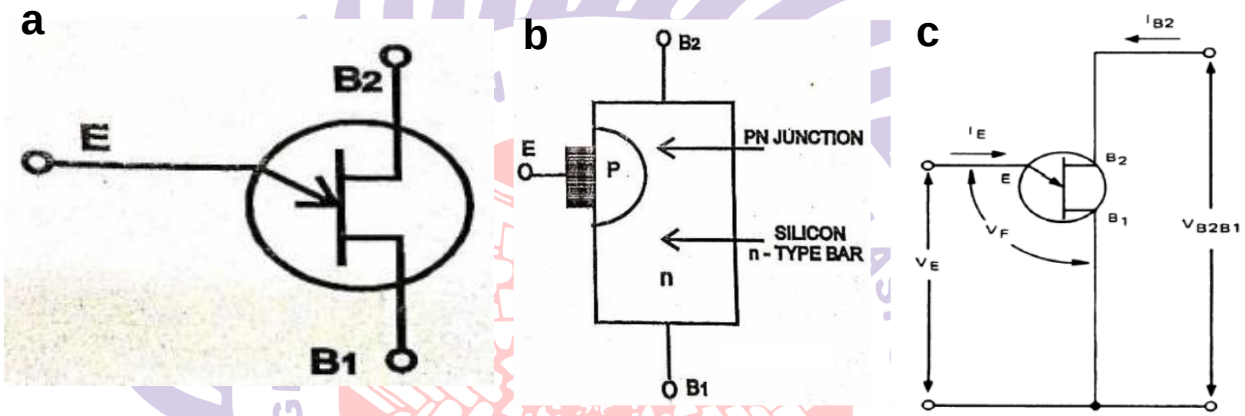

Fig 1. a Nomenclature of UJT, **b** basic structure of UJT and **c** basic Circuit of UJT

The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect is a negative resistance at the emitter terminal.

Circuit Operation:

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Fig. 2 shows the basic circuit operation of a unijunction transistor. The device is nprmally B2 positive w.r.t B1. There are two posibilities:

i. If voltage V_{BB} is applied between B1 and B2 with emitter open as shown in Fig. 2a, then a voltage gradient is established along the N type bar. Since the Emitter (E) is located nearer to B2 more than half of the V_{BB} appears between the Emitter and B1, The voltage V1 between E and B1 establishes a reverse bias on the P-N junction and the Emitter current is cut off. Of course a small leakage current flows from B2 to E due to minority carriers.

ii. If a positive voltage is applied at the Emitter as shown in Fig. 2b, the P-N junction remains reverse biased as long as the input voltage is less than V1. If the input voltage to the emitter exceeds V1, the p-N junction becomes forward biased. Under these conditions holes are injected from P-type E into N-type bar. These holes are repelled by positive B2 terminal and they are attracted towards B1 terminal of the bar. This accumulation of holes in the Emitter to B1 results in the decrease of resistance in this section of the bar. The result is that internal voltage drop from Emitter to B1 is decreased and hence the emitter current, I_E increases. As more holes are injected, a condition of saturation will eventually be reached. At this point the Emitter current is limited by the emitter voltage or emitter power supply. The device is now in the ON state. If a negative pulse is applied to the emitter, the P-N junction will be reverse biased and the Emitter is cut off. The device is then said to be in the off state.

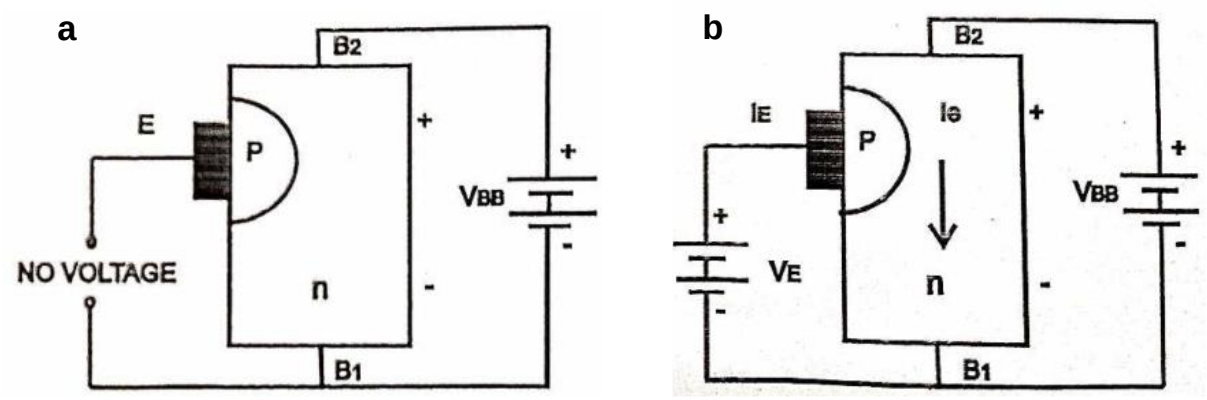

Fig. 2 Electronic circuit operation of UJT under the condition of (**a)** no applied voltage at emitter and (**b**) positive applied Voltage.

Equivalent Circuit Model:

A simplified equivalent circuit for the UJT is shown in Fig. 3. V_{BB} is a source of biasing voltage connected between B2 and B1. When the emitter is open, the total resistance from B2 to B1 is simply the resistance of the silicon bar, this is known as the 'inter base resistance R_{BB}. Since the N-channel is lightly doped, therefore R_{BB} is relatively high, typically 5 to 10K ohm. R_{B2} is the resistance between B2 and point 'a', while R_{B1} is the resistance from point 'a' to B1, therefore the interbase resistance R_{BB} is:

$R_{BB} = R_{B1} + R_{B2}$

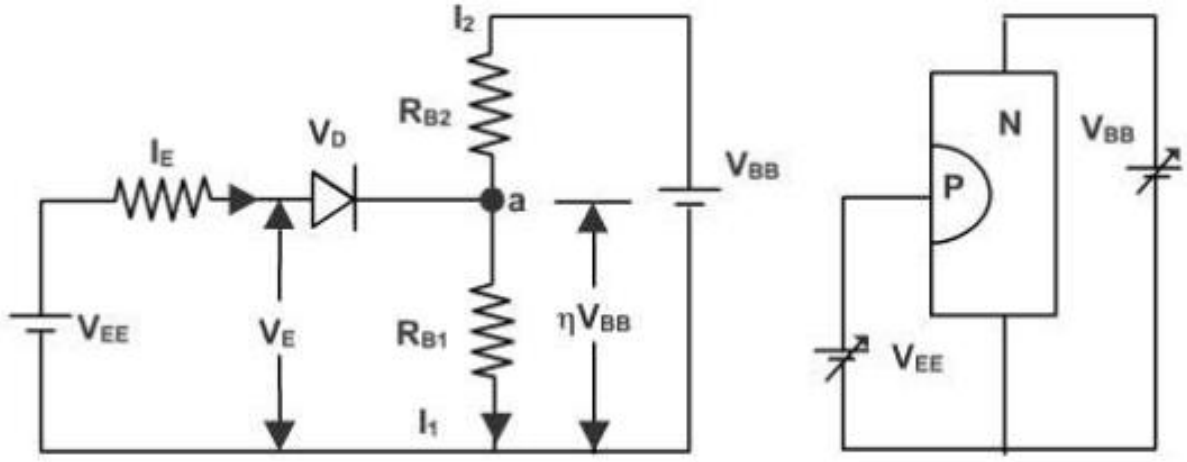

Fig. 2 Equivalent circuit of UJT.

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The diode accounts for the rectifying properties of the P-N junction. V_D is the diode's threshold voltage. With the emitter open, $I_E = 0$, and $I_1 = I_2$. The interbase current is given by:

$I_1 = I_2 = V_{BB} / R_{BB}$.

Part of V_{BB} is dropped across R_{B2} while the rest of voltage is dropped across R_{B1}. The voltage across RB1 is:

$V_a = (V_{BB} * R_{B1}) / (R_{B1} + R_{B2})$.

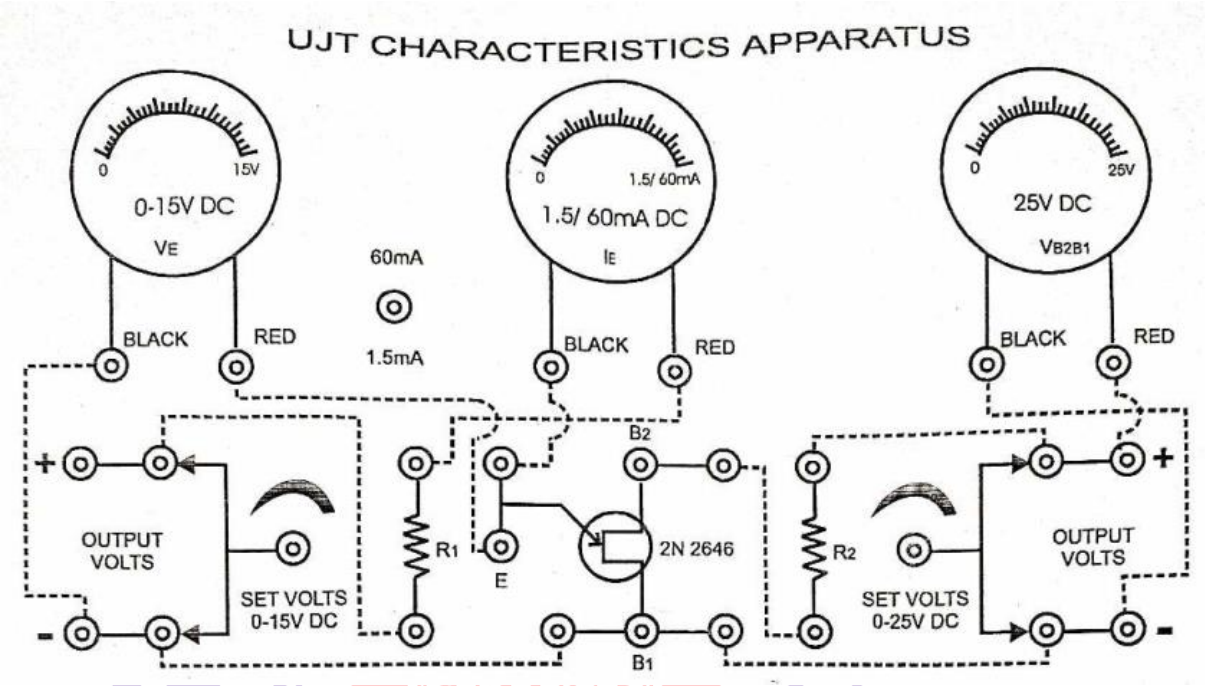
The ratio $R_{B1} / (R_{B1} + R_{B2})$ is called intrinsic standoff ratio:

$\eta = R_{B1} / (R_{B1} + R_{B2})$ i.e. $V_a = \eta V_{BB}$. The ratio η is a property of UJT and it is always less than one and usually between 0.4 and 0.85. As long as $I_B = 0$, the circuit will behave as a voltage divider.

Assume now that V_E is gradually increased from zero using an emitter supply V_{EE}. The diode remains reverse biased till V_E voltage is less than ηV_{BB} and no emitter current flows except leakage current. The emitter diode will be reversed biased. When $V_E = V_D + \eta V_{BB}$, then appreciable emitter current begins to flow where V_D is the diode's threshold voltage. The value of V_E that causes, the diode to start conducting is called the peak point voltage, V_P and the current is called peak point current I_P. $V_P = V_D + \eta V_{BB}$.

Experimental Procedure:

1. Identify the components required (power supply, voltmeter, ammeter, diode) and Connect the dotted lines through pathcodes as given in the below circuit.
2. Keep both the power supplies at zero potential.
3. Switch On the instrument using ON/OFF toggle switch provided on the front panel.
4. Select the current meter range to 1.5 mA through SPDT switch.



5. Adjust $V_{B2\,B1}$ (voltage between B2 and B1) to +5V DC.
6. Increase the value V_E (emitter voltage) in small steps and Note down the corresponding value of I_E (emitter current).
7. Now change Miliammeter range to 60 mA and starts increasing the value of V_E, at a particular Value of V_E, I_E value increases sharply with decrease in V_E. Note down the value of V_E at that instant.
8. Adjust $V_{B2\,B1}$ (voltage between B2 and B1) to different voltages such as 10V, 15V & 20V, again repeat the 6 & 7th steps.
9. Draw a plot between I_E and V_E as shown in Fig. 4.
10. From your observations obtain the value of cut-in voltage and breakdown voltage V_Z.

Observation Table:

Table:1

S. No.	$V_{B2\,B1}$ = 5 V		$V_{B2\,B1}$ = 10 V		$V_{B2\,B1}$ = 15 V		$V_{B2\,B1}$ = 20 V	
	V_E (V)	I_E (mA)	V_E (V)	I_E (mA)	V_E (V)	I_E (mA)	V_E (V)	I_E (mA)
1								

2								
3								
4								
5								
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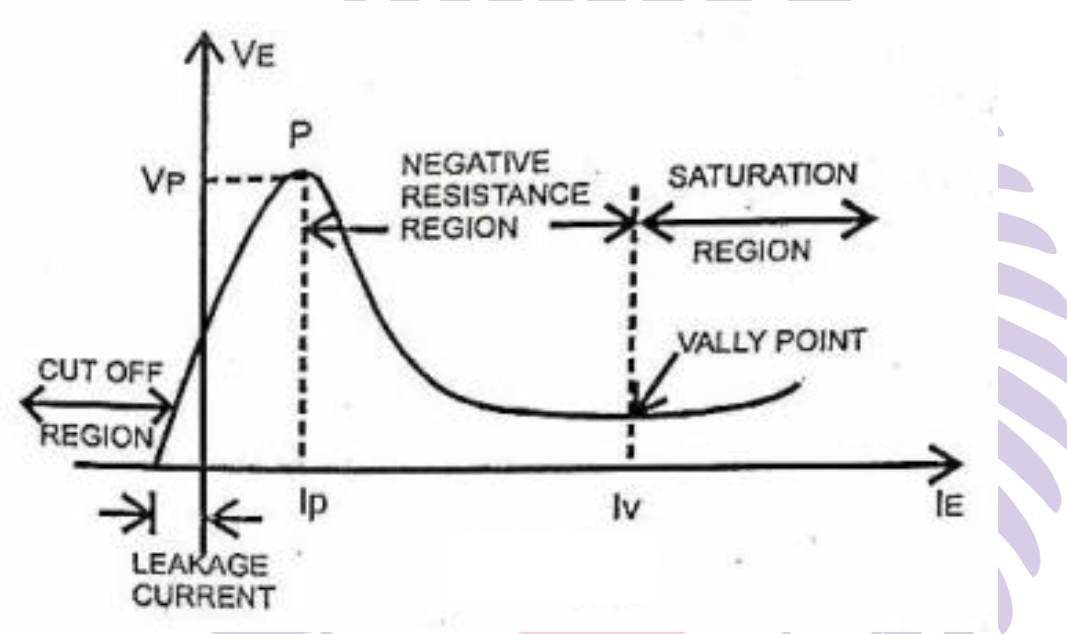
10								

Characteristics Curve:



The Above graph shows the relationship between the emitter voltage (V_E) and current (I_E) of a UJT at a given voltage V_{BB} ($V_{B2\,B1}$) between the bases where V_E is plotted on the vertical axis and I_E is plotted on the horizontal axis. This is emitter the characteristic of UJT and the following points can be concluded:

i. Initially, the region where V_E started to increase from zero is called as cut off region because no emitter current flows (except slight leakage due to the minority charge carriers in the revers biased mode).

ii. Above a certain value of V_E, forward current I_E begins to flow and increases until the peak voltage V_P and current I_P are reached at point P.

iii. After the peak point P, at attempt to increase V_E is followed by a sudden increase in emitter current, I_E with a corresponding decrease in V_E up to a certain point called valley point (V_V and I_V). This is called negative resistance region.

iv. Beyond this, I_E increases with V_E this is the saturation region, which exhibits a positive resistance characteristic.

v. The physical process responsible for the negative resistance characteristic is called conductivity modulation. When the V_E exceeds V_P voltage, holes from P emitter are injected into N base. Since the P region is heavily doped compared with the N-region, holes are injected to the lower half of the UJT. The lightly doped N region gives these holes a long lifetime. These holes move towards B1 to complete their path by re-entering at the negative terminal of V_{EE}. The large holes create a conducting path between the emitter and the lower base. These increased charge carriers represent a decrease in resistance R_{B1}, therefore can be considered as variable resistance. It decreases up to 50 ohm. Since η is a function of R_{B1} it follows that the reduction of R_{B1} causes a corresponding reduction in intrinsic standoff ratio. Thus as I_E increases, R_{B1} decreases, η decreases, and V_a decreases. The decrease in V_a causes more emitter current to flow which causes further reduction in R_{B1}, η, and V_a. This process is regenerative and therefore V_a as well as V_E quickly drops while I_E increases. Although R_B decreases in value, but it is always positive resistance. It is only the dynamic resistance between V_V and V_P. At point B, the entire base1 region will saturate with carriers and resistance R_{B1} will not decrease any more. A further increase in I_E will be followed by a voltage rise. The diode threshold voltage decreases with temperature and R_{BB} resistance increases with temperature because Si has positive temperature coefficient.

Calculation:

1. A graph is plotted between V_E and I_E for different values of V_{B2B1} and determine the V_P from the plot.
2. Intrinsic Stand-Off ratio is calculated using $\eta = (V_P - V_D) / V_{B2B1}$

Precautions:

1. Connections should be done properly.
2. Voltmeter and ammeter of appropriate ranges should be selected properly.
3. Turn off the setup box when it was used.
4. Never cross the limits specified by the manufacturer, otherwise the diode will get damaged.

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Experiment 7: Study of the I-V Characteristics of JFET

Objective:

1. To study the I-V characteristics (Drain and Transfer Characteristics) of a n-channel depletion type (BFW 10) Junction Field Effect Transistor (JFET).
2. Low frequency small signals model evaluation of Junction Field Effect Transistor (JFET).

Apparatus: Junction Field Effect Transistor (JFET) I-V Characteristics apparatus comprised of:

1. Two continuously variable DC regulated power supplies of 0-30V with output on sockets.
2. Three digital panel meters ($3^{1/2}$ digit DPM) to measure voltage & current which are mounted on front panel & connections brought out on sockets.
3. One N-Channel depletion type JFET (BFW 10) is placed behind the cabinet panel & connections are brought out on sockets.

Theory:

The Junction Field Effect Transistor (JFET) is a three-terminal device fabricated using monolithic silicon technology with one terminal (called the gate) capable of controlling the current between the other two terminals (drain and source). The primary difference between FET and BJT transistors is the fact that the BJT transistor is a current-controlled device, while the JFET transistor is a voltage-controlled device. The FET transistor is a unipolar device depending on either

electron conduction (N-channel JFET) or hole conduction (P-channel JFET). In contrast, the BJT transistor is a bipolar device, meaning that the conduction depends on two charge carriers (electrons and holes) in the same time. Another difference between two devices is the high input impedance of the JFET when compared with the BJT. The input impedance is usually larger than 1 MΩ. However, typical AC voltage gains for BJT amplifiers are greater than those for FET amplifiers. Furthermore, FETs are more temperature stable than BJTs and are usually smaller in size with longer life and high efficiency, making them particularly useful in integrated circuit chips. FET has negative temperature coefficient of resistance.

The structure, symbol and pin assignment of a JFET is given in Fig. 1. The major part of JEET is the channel between embedded P types of material. The top of the n-channel is connected to an ohmic contact called as 'Drain' (D) & lower end of Channel is called as 'Source' (S). The two p types of materials are connected together & to the 'Gate' terminal (G).

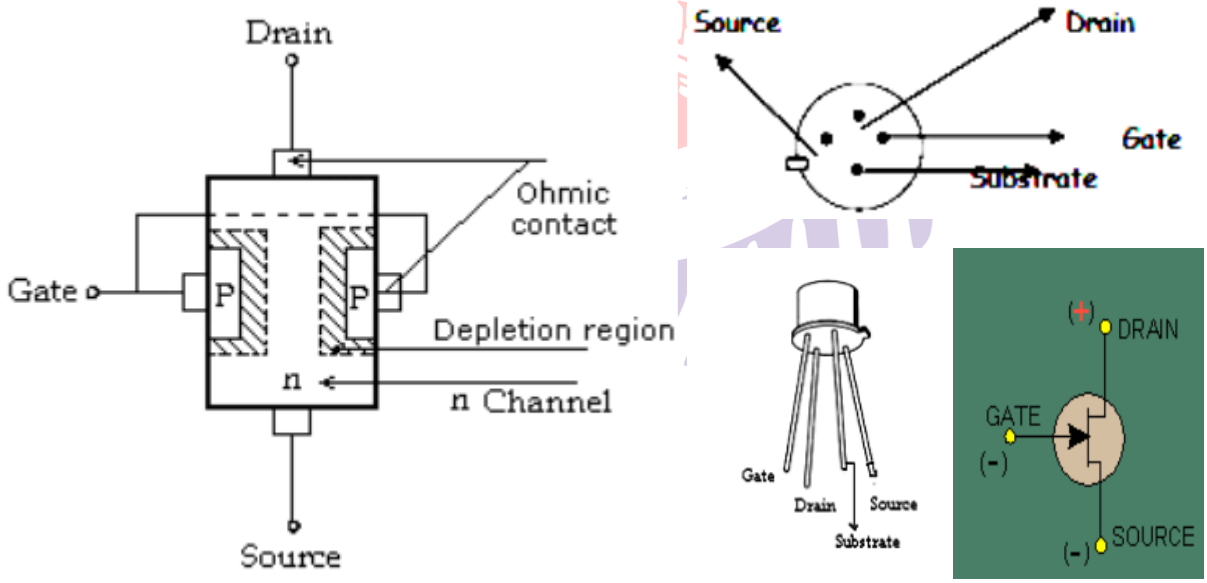

Fig 1. Basic structure, symbol and Pin assignment of a n-channel JFET.

I-V CHARACTERISTICS OF A JFET:

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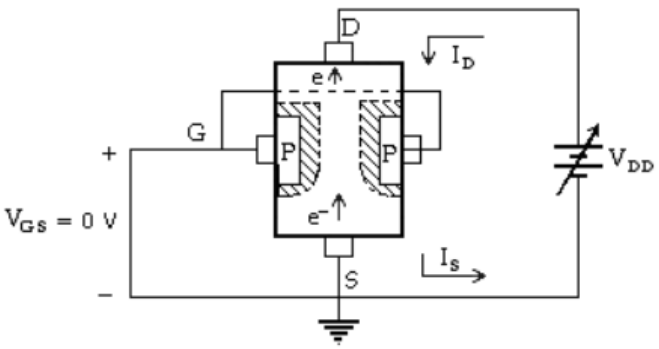
In the JFET the transistor action is determined by the flow of majority carriers between the source and the drain. In the low drain-source bias region the current flow is controlled by a voltage applied to the gate terminal that consists of a reversed biased p-n junction. The gate voltage modulates the width of the reverse biased p-n junction depletion layer. The change in the cross-sectional area of the current path under the gate modulates the current flow. For a fixed source-drain voltage and with increasing gate bias the width of the depletion layer at the drain end of the channel decreases. The most important operating region of the JFET occurs at larger drain-source bias levels. There the combination of the applied gate voltage and the drain to source voltages are sufficiently large so the depletion width extends fully across the channel, pinching it off at the drain end of the channel. The current flow is now limited by the current flow in the non-pinched off region of the channel, and when the carriers reach the pinched off end they are rapidly collected by the reverse bias of the pinched off region. Analysis of the device geometry shows that in the pinched off region the current flow is determined by the value of the gate voltage, and is relatively independent of the drain-source voltage. This is the practical region for operating the JFET as an amplifier.

The DC behavior of a JFET is specified depending on different conditions which are elaborated below:

1. V_{GS} = 0V, V_{DS} is some +ve value:



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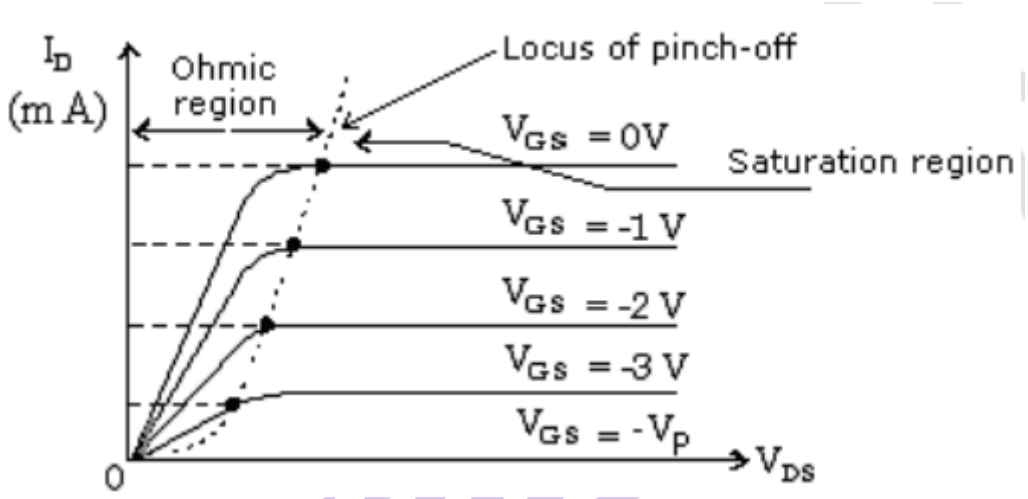
As shown in the above figure the gate is directly connected to source to achieve V_{GS} = 0V, this is similar to no bias condition. The instant the voltage V_{DD} (=V_{DS}) is applied, the electrons will be drawn to the drain terminal, causing I_D & I_S to flow (i.e. I_D = I_S). Under this condition the flow of charge is limited solely by resistance of the n channel between drain & source. It is important to note that the depletion region wider at the top of both p type of material. Since the upper terminal is more reverse bias than the lower terminal (source - S).

As voltage V_{DS} is increased from 0 to few volts, the current will increase as determined by ohm's law. If still V_{DS} is increased & approaches a level referred as V_P, the depletion region will widen, causing a noticeable reduction in channel width. The reduced path of conduction causes the resistance to increase. The more the horizontal curve, the higher resistance. If V_{DS} is increase to a level where it appears that the two-depletion region would touch each other, the condition referred as 'pinch–off' will result. The level of V_{DS} that establish this condition is called as 'pinch off voltage' (V_P). At V_P, I_D should be zero, but practically a small channel still exists & very high density current still flows through the channel. As V_{DS} is increased beyond V_P, the saturation current will flow through the channel (i.e I_{DSS}) where I_{DSS} = Drain to source current with short cut connection from source to Gate.

2. V_{GS} < 0V:

If a –ve bias is applied between gate and source, the effect of the applied –ve bias V_{GS} is to establish depletion region similar to those obtained with V_{GS} = 0V but at lower level of V_{DS}. As V_{GS} will become more & more –ve biased, the depletion layer pinch off occur at the less & less value of V_{DS}. Eventually, when V_{GS} = -V_P, will be sufficiently –ve to establish a saturation level, i.e. essentially 0 mA & for all practical purpose the device has been 'turned OFF' as shown in below figure.



The region to the right of the pinch–off locus is typically employed in linear amplifiers (Amplifier with minimum distortion at applied signal) is commonly referred as the constant current, saturation or linear amplification region.

3. Voltage controlled region:

The region left of pinch–off locus is called as ohmic or voltage-controlled region. In this region the JEET can actually be employed as a variable register whose resistance is controlled by V_{GS}. As V_{GS} becomes more & more –ve, the slope of the curve becomes more and more horizontal, corresponding with an increasing resistance level. The resistance (r_d) at particular value of V_{GS} is given by:

$$r_d = \frac{r_0}{\left(1-\frac{V_{GS}}{V_P}\right)^2}$$, where r_o is the resistance with V_{GS} = 0V.

4. Drain and Transfer characteristics:

DC behaviour of JFET is most completely controlled by the output characteristics or drain chracteristics, I_D versus V_{DS}, with V_{GS} as a parameter, as shown in Fig. 2a, and the input-output characteristic or transfer characteristics, I_D versus V_{GS}, as shown in Fig. 2b.

The drain current (I_D) of the JFET is controlled by the application of reverse-biased voltage between gate and source terminals (V_{GS}). The relationship between I_D and V_{GS} is defined by the well-known Shockley's equation:

$$I_d = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Where V_P is called the pinch-off voltage and I_{DSS} is known as the drain saturation current. When $V_{GS} = V_P$ then $I_D = 0$, and the FET is in the cut-off region. Shockley's Equation indicates that the FET is a square-law device.

The transfer characteristic of the JFET is obtained by varying the negative voltage V_{GS} between V_P and 0 and measuring I_D for a given value of the drain to source voltage (V_{DS}).

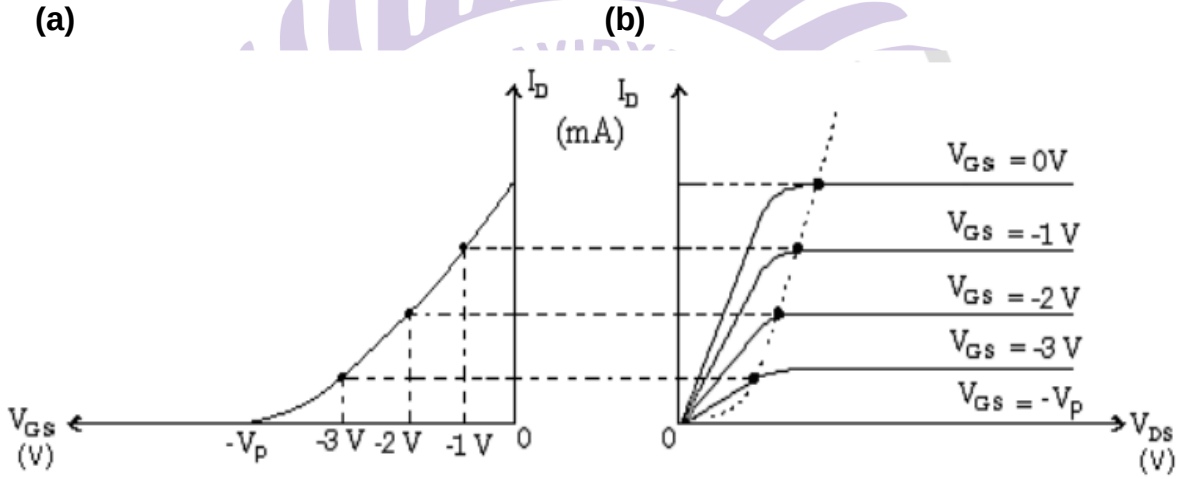


Fig. 2 (a) Transfer and **(b)** Drain characteristics of a JFET.

JFET Parametrs:

1. Drain Resistance (r_d): It is given by the relation of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in Drain Current (ΔI_D) for a constant gate to source voltage (ΔV_{GS}), when the JFET is operating in pinch-off region, then $r_d = \Delta V_{DS} / \Delta I_D$ at a constant V_{GS} (from drain characteristics)

2. Trans Conductance/Transductance (g_m): Ratio of small change in drain current (ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant V_{DS}.

$g_m = \Delta I_D / \Delta V_{GS}$ at constant V_{DS} (from transfer characteristics).

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The value of g_m is expressed in mho's (℧) or Siemens (s).

4. Amplification factor (μ): It is given by the ratio of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant drain current (I_D).

$$\boldsymbol{\mu} = (\Delta \boldsymbol{V_{DS}}/\Delta \boldsymbol{I_D}) \times (\Delta \boldsymbol{I_D}/\Delta \boldsymbol{V_{GS}}) = \Delta \boldsymbol{V_{DS}}/\Delta \boldsymbol{V_{GS}} \; ie. \; \boldsymbol{\mu} = \boldsymbol{r_d} \times \boldsymbol{g_m}$$

Small Signal Model:

The small signal equivalent circuit of a JFET operating in the pinched-off mode is shown in Fig. 3. When used as a small signal amplifier the JFET will be operating in the pinched-off mode, $V_{DS} > |V_{GS} - V_P| > 0$, and its DC behavior can be approximately described by the following equation: $I_d = I_{DSS}\left(1 + \frac{V_{GS}}{V_P}\right)^2$ *for negative* V_{GS}.

The transconductance is gm and is equal to the slope of the transfer curve in Fig. 2 which is given by:

$$g_m = \left(\frac{\partial i_D}{\partial v_{GS}}\right)\Big|_{v_{DS}=const.} = \left(\frac{\Delta i_D}{\Delta v_{GS}}\right)\Big|_{v_{DS}=const.}$$

Eqn. This equation can be $g_m = \left(\frac{-2I_{DSS}}{V_p}\right)\left(1 + \frac{v_{GS}}{V_P}\right)$ rearranged as:

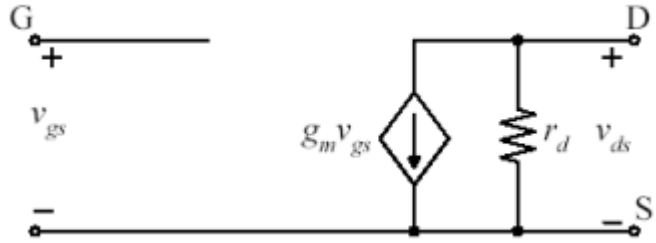

Fig. 3. The small signal model of a JFET in the pinched off mode of operation.

g_m is evaluated at a fixed value $v_{GS} = V_{GS}$. The input terminals from the gate to the source appear as a reversed biased diode and are an effective open circuit. The

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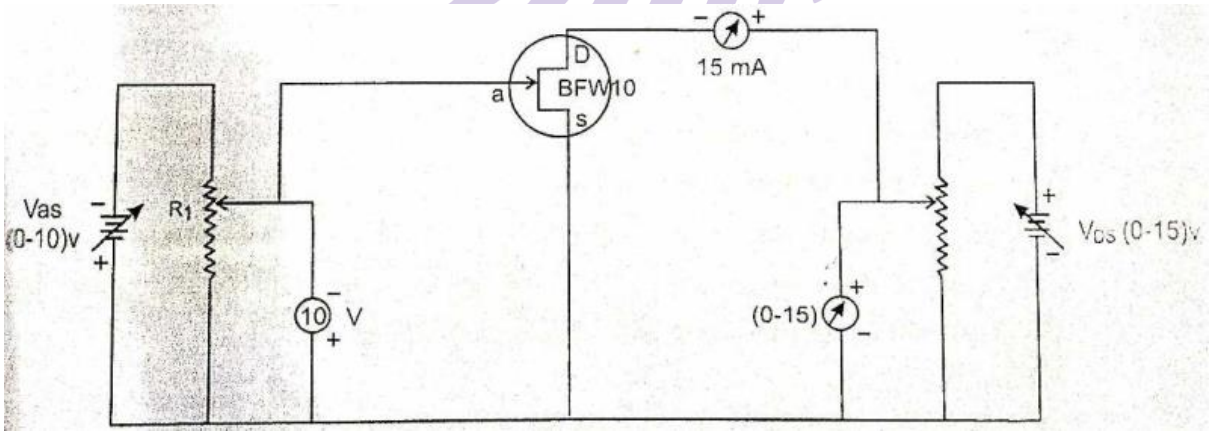
numerical value of g_m can be estimated from above equation or from Fig. 2b. The latter approach will be used in this experiment. To find g_m from the characteristic curves of Fig. 2b, find the desired operating point (i_D, v_{DS}) that is determined by the load resistor and the drain supply voltage v_{DD}. Then, draw a vertical line through the v_{DS} operating point. On this line find the voltage difference between the two nearby characteristic curves, Δv_{GS}. Extrapolate the two intersection points to the y-axis and find Δi_{DS}. Then use first equation of this section to find g_m. The output resistance r_d shunting the $g_m v_{GS}$ current generator is included in the model to account for changes in the drain current due to changes in v_{DS}. The numerical value of r_d can be obtained from the slope of the I_D vs V_{DS} curve above saturation in Fig. 2b or from a small signal AC measurement at the desired DC operating point. The value of r d is inversely proportional to the change in the DC value of the drain current. Use the following graphical analysis to obtain r_d. Find the characteristic curve closest to the operating point and draw a straight line superimposed on the saturation part of the curve. Select two convenient values of v_{DS} and draw two vertical lines through these points to where they intersect the straight curve. Circle the intersection points. The x-axis separation gives the value Δv_{DS}. Next draw horizontal lines through the circles to the y-axis. The y-axis separation gives the value of Δi_D. The value of $r_d=(\Delta v_{DS}/\Delta i_D)$.

Test Circuit for JFET Characteristics:



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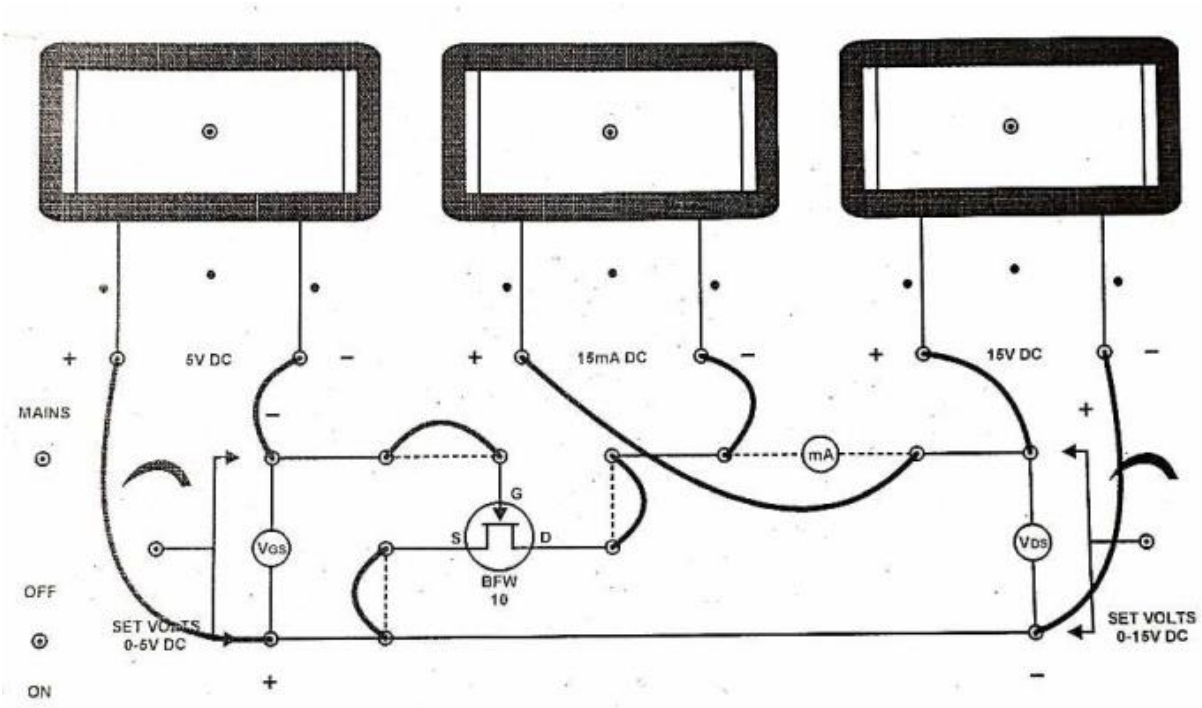
Experimental Procedure:

OUTPUT CHARACTERISTICS:

1. Connect the circuit properly as per given diagram below.



2. Switch on the apparatus using ON/OFF toggle switch provided on the front panel.
3. Keep V_{GS} = 0V by varying V_{GG}.
4. Initially Keep V_{DS} to 0 Volts.
5. Vary VDS in step of 0.5V up to 12 volts and note down the corresponding drain current I_D.
6. Repeat the above procedure for Keeping V_{GS} as -0.5, -1V, -1.5V, -2V, -2.5V, -3V, -3.5V etc and tabulate all the readings.
7. Plot a graph between V_{DS} and I_D for different values of V_{GS} by taking V_{DS} along x-axis and ID along y-axis.

TRANSFER CHARACTERISTICS:

1. Adjust V_{GS} to 0 volts and follow the steps 4 & 5 on the same circuit.

2. Set the voltage V_{DS} constant at 10 V. Vary V_{GS} by varying V_{GG} in the step of 0.5 up to 3.5V and note down value of drain current I_D. At particular value of V_{GS} voltage, drain current reduces to Zero V_{GS} (OFF). The Gate voltage at which the channel is cut-off is called Gate Source cut-off voltage.
3. Tabulate all the readings.
4. Plot the transfer characteristics V_{GS} vs I_D.
5. Calculate I_{DSS}, V_P, g_m, r_d or r_o from the graphs and verify it from the data sheet.

Observation Table:

Table:1 OUTPUT CHARACTERISTICS

S. No.	V_{GS} = 0 V		V_{GS} = -0.5 V		V_{GS} = -1 V		V_{GS} = -1.5 V… upto -3.5 V	
	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								

Table:2 TRANSFER CHARACTERISTICS

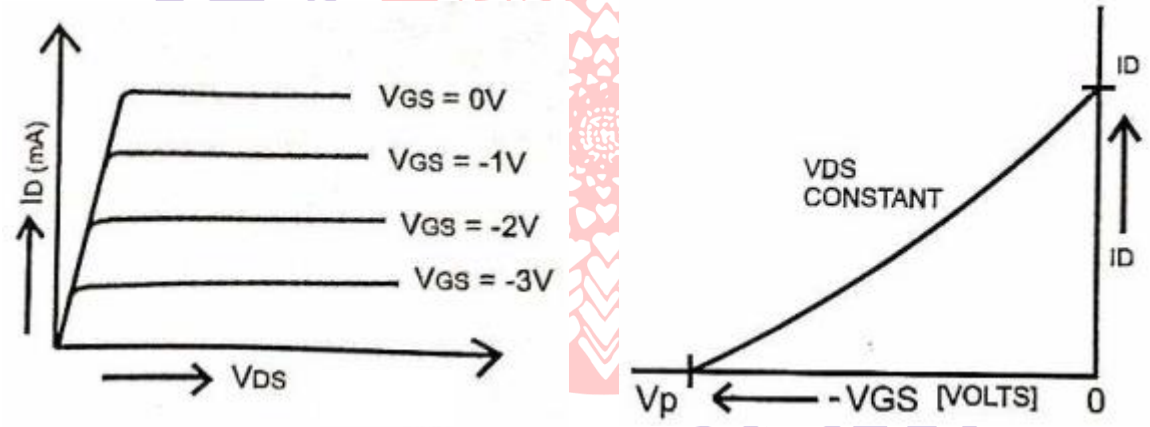
S. No.	V_{DS} = 10 V		V_{DS} = 15 V	
	V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)
1				
2				
3				
4				
5				

6				
7				
8				
9				
10				

Table:3 FOR PINCH OFF VOLTAGE

S. No.	Gate source voltage (V)	Pinch off voltage
1	At volts	
2	At volts	
3	At volts	
4	At volts	

Model Plot:



Calculation:

1. Drain saturation current I_{DSS}: Maximum current flowing through JFET when gate to source voltage is zero.
2. Pinch-off voltage V_P: Gate to source voltage at which, drain current becomes zero.
3. Transconductance g_m: Ratio of small change in drain current (ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant V_{DS}.
   $g_m = (\Delta I_D/\Delta V_{GS})$ at constant V_{DS}

4. Output resistance : It is given by the relation of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in Drain Current (ΔI_D) for a constant V_{GS}, when the JFET is operating in pinch-off region.

   r_d or $r_o = (\Delta V_{DS} / \Delta I_D)$ at a constant V_{GS}.

Results:

1. I_{DSS} : _____

2. V_P : _____

3. g_m : _____

4. r_o : _____

Precautions:

1. Connections should be done properly.
2. Voltmeter and ammeter of appropriate ranges should be selected properly.
3. Turn off the setup apparatus when it was used.
4. Never cross the limits specified by the manufacturer, otherwise the diode will get damaged.

Appendix:

Table 1: Chart of symbols will be used in this experiment

Symbol	Symbol Name	Units
i_{DS}	total drain to source current	mA
I_{DS}	DC drain to source current	mA
i_{ds}	AC drain to source current	mA
I_{DSS}	saturation current w/ $V_G = 0$	mA
V_P	pinch off Voltage	V
v_{DS}	total drain to source voltage	V
V_{DS}	DC drain to source Voltage	V
v_{ds}	AC drain to source Voltage	V
v_{GS}	total gate to source Voltage	V
V_{GS}	DC gate to source Voltage	V
v_{gs}	AC gate to source Voltage	V
g_m	transconductance	A/V

Table 2: Chart of equations will be used in this experiment

Equation	Name	Formula
1	Saturation Drain to Source current in a N-type JFET	$I_{D(Sat.)} = I_{DSS}\left(1+\frac{v_{GS}}{V_p}\right)^2$ for negative V_{GS}
2	Transconductance at the operating point	$g_m = \left(\frac{\partial i_{DS}}{\partial v_{GS}}\right)\Big\|_{v_{DS}=const.} = \left(\frac{\Delta I_{DS}}{\Delta V_{GS}}\right)\Big\|_{v_{DS}=const.}$
3	Equation for Transconductance at the operating point using known variables	$g_m = \left(\frac{-2I_{DSS}}{V_p}\right)\left(1+\frac{v_{GS}}{V_p}\right)$
4	Total Drain to Source current	$i_{DSAT}(t) = I_{DS}(0) + \frac{I_{DSS}}{2}\left(\frac{v_{gs}}{V_p}\right)^2$ $-2I_{DSS}\left(1+\frac{v_{gs}}{V_p}\right)\frac{v_{gs}}{V_p}\cos(wt) + \frac{I_{DSS}}{2}\left(\frac{v_{gs}}{V_p}\right)^2\cos(2wt)$
5	Shift in DC operating point due to AC gate Voltage	$\Delta I_{DS} = \frac{I_{DSS}}{2}\left(\frac{v_{gs}}{V_p}\right)^2$

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Condensed Matter Physics Practical Experiment Manual

Experiment 8: Study of the I-V Characteristics of MOSFET

Objective:

1. To understand the operation of the MOSFET and determine the threshold voltage.

2. To measure the I-V characteristics and find the different operating regions.

3. To obtain MOSFET transfer characteristic curves.

Apparatus: Junction Field Effect Transistor (JFET) I-V Characteristics apparatus comprised of:

1. Two continuously variable DC regulated power supplies of 0-30V with output on sockets.
2. Three digital panel meters ($3^{1/2}$ digit DPM) to measure voltage & current which are mounted on front panel & connections brought out on sockets.
3. One N-Channel enhancemnet type MOSFET (IRF 840) is placed behind the cabinet panel & connections are brought out on sockets.

Introduction: A MOSFET transistor is a three terminal semiconductor device in which, current flowing from the drain- source terminals, is controlled by the voltage on the gate terminal and it can be used as an amplifier and a switch. The most common transistor types are the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and the Bipolar Junction Transistors (BJT). BJTs based circuits dominated the electronics market in the 1960's and 1970's. Nowadays most electronic circuits, particularly integrated circuits (ICs), are made of

MOSFETs. The BJTs are mainly used for specific applications like analog circuits (e.g. amplifiers), high-speed circuits or power electronics. There are two main differences between BJTs and FETs. The first is that FETs are charge-controlled devices while BJTs are current controlled devices. The second difference is that the input impedance of the FETs is very high while that of BJT is relatively low. As for the FET transistors, there are two main types: the junction field effect transistor (JFET) and the metal oxide semiconductor field effect transistor (MOSFET). The power dissipation of a JFET is high in comparison to MOSFETs. Therefore, JFETs are less important if it comes to the realization of ICs, where transistors are densely packed. The power dissipation of a JFET based circuit would be simply too high. MOSFETs became the most popular field effect device in the 1980's. Its major advantage over BJT in switching is that it is much more power efficient at high-frequency switching. It has a +ve temperature coefficient, so it is thermally stable. The combination of n-type and p-type MOSFETs allow for the realization of the Complementary Metal Oxide Semiconductor (CMOS) technology, which is nowadays the most important technology in electronics. All microprocessors and memory products are based on CMOS technology. The very low power dissipation of CMOS circuits allows for the integration of millions of transistors on a single chip. In this experiment, we will concentrate on the MOSFET transistor.

Theory:

The MOSFETs are the most widely used FETs. Strictly speaking, MOSFET devices belong to the group of Insulated Gate Field Effect Transistor (IGFETs). As the name implies, the gate is insulated from the channel by an insulator. In most of the cases, the insulator is formed by a silicon dioxide (SiO_2) which leads to the term MOSFET. MOSETs like all other IGFETs has three terminals, which are called Gate (G), Source (S), and Drain (D). In certain cases, the transistors have a fourth terminal, which is called the bulk or the body terminal. In PMOS,

the body terminal is held at the most positive voltage in the circuit and in NMOS, it is held at the most negative voltage in the circuit.

There are four types of MOSFETs: enhancement n-type MOSFET, enhancement p-type MOSFET, depletion n-type MOSFET, and depletion p-type MOSFET. The type depends whether the channel between the drain and source is an induced channel or the channel is physically implemented and whether the current owing in the channel is an electron current or a hole current. If the channel between the drain and the source is an induced channel, the transistor is called enhancement transistor. If the channel between the drain and source is physically implemented then the transistor is called depletion transistor. If the current owing in the channel is an electron current, the transistor is called an n- type or NMOS transistor. If the current flow is a hole current then the transistor is called p-type or PMOS transistor. Throughout here, we will concentrate on analysing the enhancement type MOSFET. The structure of an enhancement NMOS transistor is shown in Fig. 1. On to a lightly doped P-type substrate two heavily doped N-regions, separated by about 25 μm, are diffused. These N-type regions will act as the source and the drain. A thin layer of insulation Silicon dioxide is then grown over this surface and holes are cut into the oxide layer through which metal (Al) contacts for the source and drain are made. A conducting layer of aluminium which will act as gate, is overlaid on SiO_2 over the entire channel region. Because of the presence of the insulating layer of silicon dioxide this device is called the insulated-gate field effect transistor (IGFET). The semiconductor channel, the insulation dielectric SiO_2 layer and the metal layer of the gate, forms a parallel plate capacitor. The insulating layer between the gate and the channel results in an extremely high resistance (10^{10} to 10^{15} Ω) for this device.

NOTE 1: **In n-channel enhancement type MOSFET, Gate is never be operated with negative voltage.**

2. There is no I_{DSS} parameter in n-type enhancement MOSFET.

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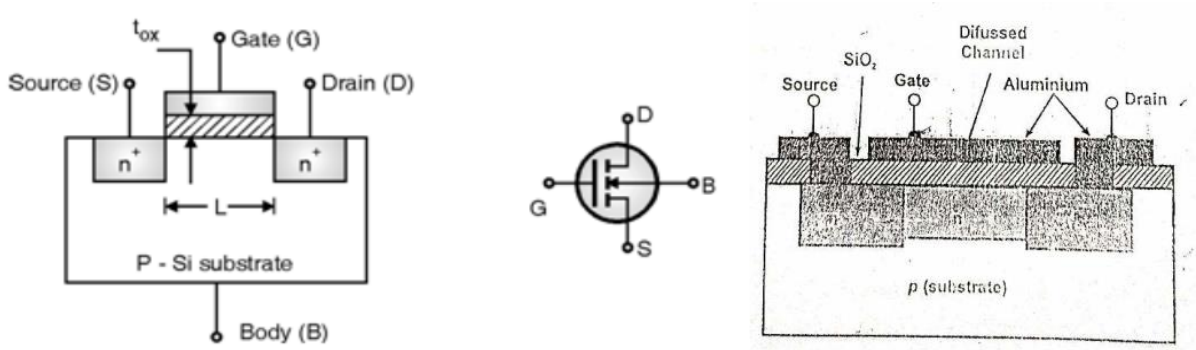

Fig 1. Cross-sectional view, symbol and basic structure of a n-channel enhancement type MOSFET.

Now, If we put the drain and source on ground potential and apply a positive voltage to the gate, the free holes (positive charges) are repelled from the region of the substrate under the gate (channel region) due to the positive voltage applied to the gate. The holes are pushed away downwards into the substrate leaving behind a depletion region. At the same time, the positive gate voltage attracts electrons into the channel region. When the concentration of electrons near the surface of the substrate under the gate is higher than the concentration of holes, an n region is created, connecting the source and the drain regions. The induced n-region thus forms the channel for current flow from drain to source. The channel is only a few nanometers wide. Nevertheless, the entire current transport occurs in this thin channel between drain and source. Now if a voltage is applied between drain and source electrodes an electron current can flow through the induced channel. Increasing the voltage applied to the gate above a certain threshold voltage enhances the channel. In the case of an enhancement type NMOS transistor the threshold voltage is positive, whereas an enhancement type PMOS transistor has a negative threshold voltage. So, in order for the current to flow from drain to source, the condition that should be satisfied is $V_G > V_{th}$, where V_G is the gate voltage and V_{th} is the minimum voltage required to form a channel between drain and source so that carriers can go through the channel. By

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changing the applied gate voltage, we can modulate the conductance of the channel.

N-channel formation and Pinch-off phenomena:

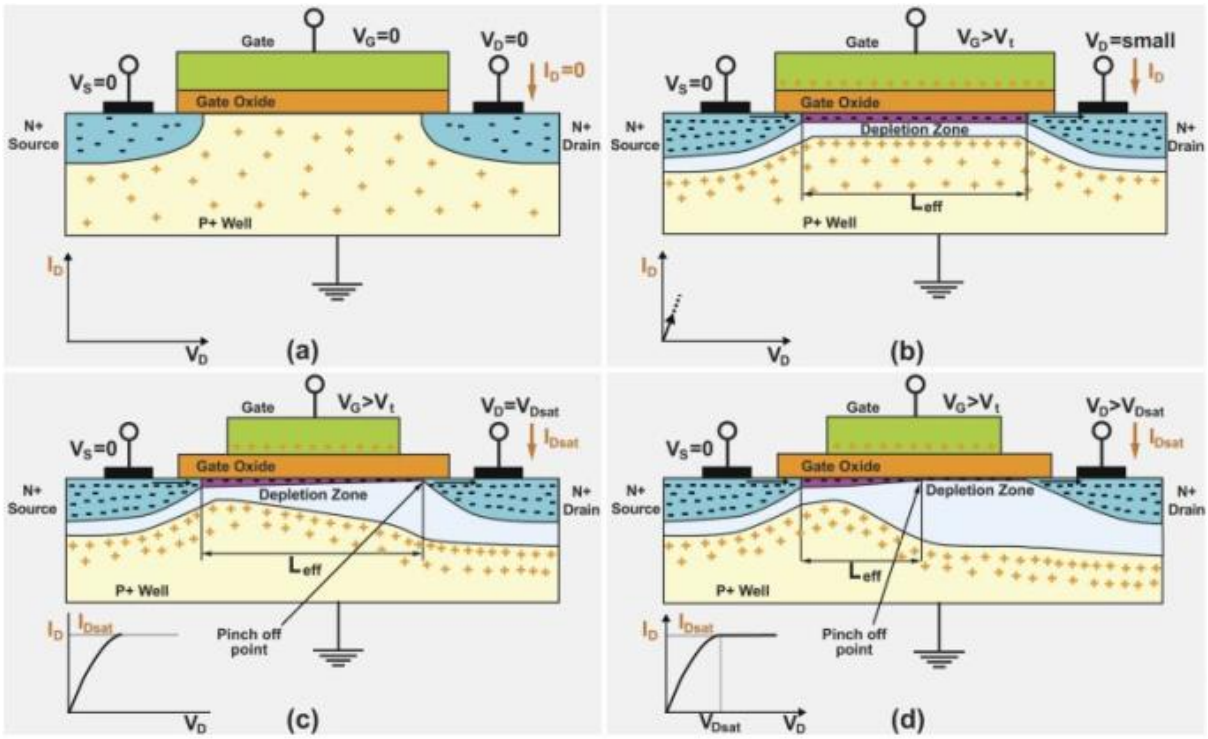

Fig 2 (a) $V_G = 0$, no biasing between Gate & Source, **(b)** $V_G > V_t$, forward bias to Gate w.r.t to Source. The -ve charge is pulled towards Gate. Thus, at a particular point number of electrons > number of holes within the depletion region. So, there is a creation of a region where n-type conductivity opposed to p-type is formed. This is called the inversion region. Hence n-channel is formed through which electrons can flow, **(c)** $VD = V_{DSat} = V_{GS} - V_t$, transition from ohmic region to saturation region and **(d)** $V_D > V_{DSat}$, pinch-off point moves towards the Source thus reducing the channel length. Under these conditions, the area between the pinch-off point and the drain is fully depleted with no inversion layer. Since this region has no positive free carriers, there is no possibility for electron-hole recombination if an electron enters the region from the electron-rich source and, if there is an electric field across the depletion zone, the electron can freely transit

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to the drain. The current through the device becomes controlled solely by the gate voltage under drain saturation conditions.

Threshold voltage and Drain Characteristics of a MOSFET:

Threshold Voltage (V_{TH} or V_{TN}):

Threshold voltage, for an enhancement-type MOSFET, is the minimum amount of gate-to-source voltage which must be applied to create an inversion region for the conduction of charge carriers across the device, between the drain and the source, on the application of suitable bias between them (see Fig. 3).

Transconductance (g_m or K_n):

It is the ratio of the current change at the output port to the voltage change at the input port as depicted in Fig. 3.

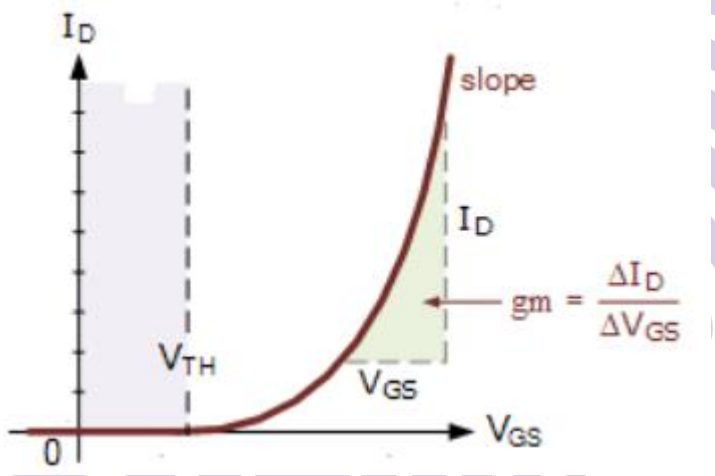

Fig. 3 Threshold voltage (VTH) and transconductance (gm) of the MOSFET device.

Drain and Transfer characteristics:

A) Ohmic/triode region: $I_D = k[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2]$

for small values of V_{DS}, ID = $I_D = k[2(V_{GS} - V_{TH})V_{DS}]$

$I_D \propto V_{DS}$ (linear)

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B) Saturation region:

$V_{DS} \geq (V_{GS} - V_T)$

$I_D \neq f(V_{DS})$ (almost true)

C) Cut-off region:

$V_{GS} < V_T$

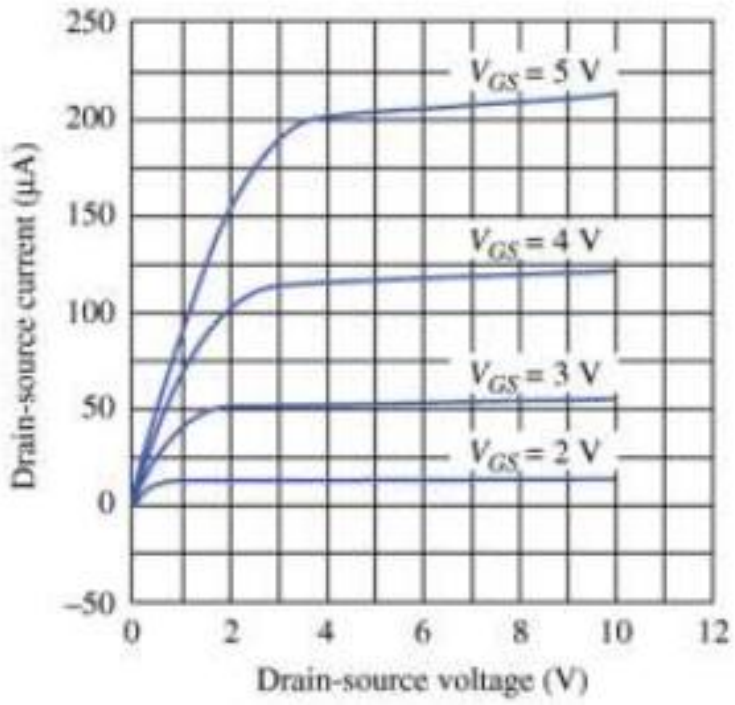
$I_D = 0$ (Device is OFF)

Table 1. Mathematical model of the n-channel MOSFET.

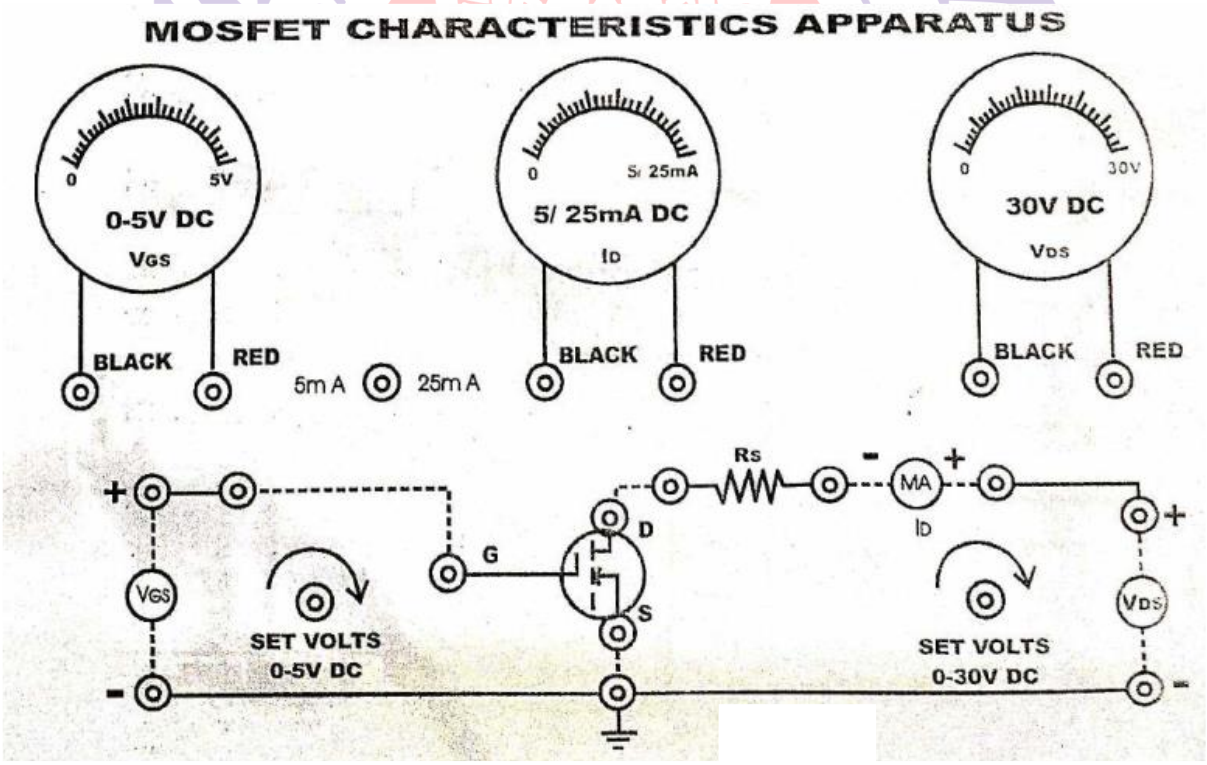
Region	Condition(s)	Equation(s)
All		$i_G = 0 \quad i_B = 0$
Cutoff	$v_{GS} \leq V_{TN}$	$i_D = 0$
Triode (Linear)	$v_{GS} - V_{TN} \geq v_{DS} \geq 0$	$i_D = K_n(v_{GS} - V_{TN} - \frac{v_{DS}}{2})v_{DS}$
Saturation	$v_{DS} \geq (v_{GS} - V_{TN}) \geq 0$	$i_D = \frac{K_n}{2}(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})$

λ is the channel length modulation parameter. It determines the slope of the MOSFET curves in saturation. For an ideal device, λ is zero.

- The output characteristics of a MOSFET with V_{TN} = 1 V, K_n = 12.5 μA/V_2, and λ = 0.325 are shown in below figure.



Test Circuit for MOSFET Characteristics:



Experimental Procedure:

Transfer Characteristics:

1. Connect the circuit properly as per given diagram above.

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2. Keep the control knobs of both the power supplies anticlockwise and switch on the instrument by changing the position of toggle switch ON side provide on the front panel. LED provided on the front panel will glow indicating theat instrument is ready to use.
3. Set the voltage V_{DS} constant at 15 V.
4. Keep V_{GS} at 0.5V and note down the drain current.
5. Vary V_{GS} in the step of 0.5 up to 3.5V and note down value of drain current I_D.
6. Tabulate all the readings.
7. Plot the transfer characteristics V_{GS} vs I_D.
8. Calculate V_{Th} and g_m from the graphs and verify it from the data sheet.

Drain Characteristics:

1. Keep V_{GS} (Gate to Source voltage) constant at 2.9V (>V_{TH} say V_{TH} + 0.1 V) on the same circuit.
2. Initially Keep V_{DS} (Drain to Source voltage) at 0.5 Volts and not down the corresponding Drain current.
3. Vary VDS in step of 0.5V up to 12 volts and note down the corresponding drain current I_D.
4. Repeat the above procedure for Keeping V_{GS} as 2.95V, 3.0V, etc and tabulate all the readings.
5. Plot a graph between V_{DS} and I_D for different values of V_{GS} by taking V_{DS} along x-axis and ID along y-axis.

Observation Table:

Table:1 TRANSFER CHARACTERISTICS

S. No.	V_{DS} = 15 V		V_{DS} = 20 V	
	V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)
1				
2				

3				
4				
5				
6				
7				
8				
9				
10				

Table:2 Drain CHARACTERISTICS

S. No.	$V_{GS} = V_{TH}$ +0.1 V		$V_{GS} = V_{TH}$ +0.3 V		$V_{GS} = V_{TH}$ +0.5 V		$V_{GS} = V_{TH}$ +0.7 V … upto V_{TH} +1.1	
	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								

Calculation:

A. Plot the transfer characteristics curve (I_{DS} vs V_{GS}).

B. Calculate the transconductance and write the threshold voltage

C. Plot the drain characteristics curve indicating –

a) Pinch-off points

b) Ohmic/triode region

c) Saturation region

For all V_{GS}

2) Calculate $R_{DS}(ON)$ for different V_{GS}.

Plot R_{DS} vs V_{GS}. Does it increase or decrease on increasing VGS and why?

Results:

1. V_{TH} : _____

2. g_m : _____

3. R_{DS} : _____

Precautions:

1. Connections should be done properly.
2. Voltmeter and ammeter of appropriate ranges should be selected properly.
3. Turn off the setup apparatus when it was used.
4. Never cross the limits specified by the manufacturer, otherwise the diode will get damaged.