DEPARTMENT OF PURE & APPLIED PHYSICS

LAB MANUAL

On

Analog System and Application Lab

B.Sc. 3rd Semester (Physics)

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Bilaspur-495009, Chhattisgarh, India

DEPARTMENT OF PURE AND APPLIED PHYSICS

B.Sc.(Physics)

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SEMESTER-III

Core-7 : Analog System and Applications Lab

LIST OF EXPERIMENTS

1. **To study V-I characteristics of PN-junction diode.**
2. **To study V-I characteristics of Zener diode and its use as voltage regulator.**
3. **Study of V-I and power curves of solar cells, and find its maximum power point & efficiency.**
4. **To study the characteristics of a Bipolar Junction Transistor (PNP) in CE configuration.**
5. **To study the characteristics of a Bipolar Junction Transistor (NPN) in CE configuration.**
6. **To study the Colpitt's oscillator.**
7. **To study the Hartley's oscillator.**

References: The content of manual are taken from Internet.

EXPERIMENT NO. – 01

- **OBJECTIVE:-** To study V-I characteristics of PN-junction diode.

- **APPARATUS REQUIRED:-** Semiconductor P-N junction diode kit and connecting wires.

- **THEORY AND FORMULA USED:-** A Semiconductor diode is prepared by joining P and N sections of a semi conducting material like germanium or silicon. The P type has excess number of holes while the N type has excess number of electrons. Holes and electrons are respectively the charge carriers in P and N type. They are called the majority carriers. Near about the junction, holes and electrons recombine giving rise to a charge free space called depletion region or barrier region. In this Process, + ve charge gets accumulated at the barrier of the N section, and - ve charge at the barrier of the P section, creating a potential barrier. A sort of a fictitious battery with it's + ve pole on the N section and - ve pole on the P section is formed. This barrier stops further motion of holes towards N side and electrons towards P side.

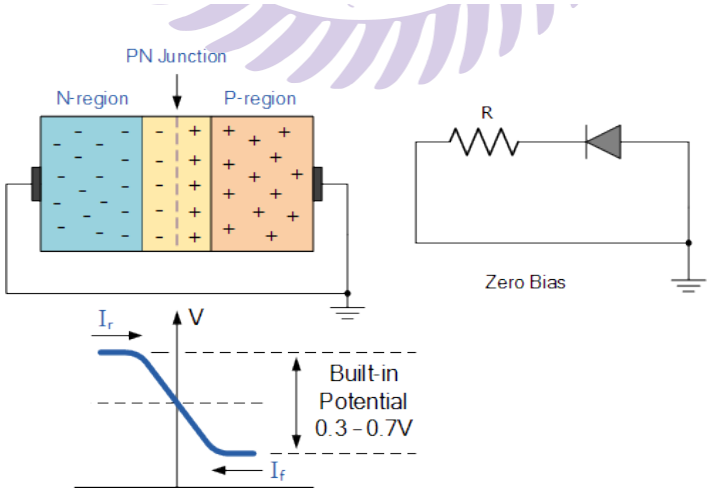


Figure 1. PN-Junction diode

i. **Forward Biasing-** When P-type (Anode is connected to +ve terminal and n-type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. On forward biasing, initially no current flows due to barrier potential. As the applied potential exceeds the barrier potential the charge carriers gain sufficient energy to cross the potential barrier and hence enter the other region. The holes, which are majority carriers in the P-region, become minority carriers on entering the N-regions, and electrons, which are the majority carriers in the N-region, become minority carriers on entering the P-region. This injection of Minority carriers results in the current flow, opposite to the direction of electron movement.

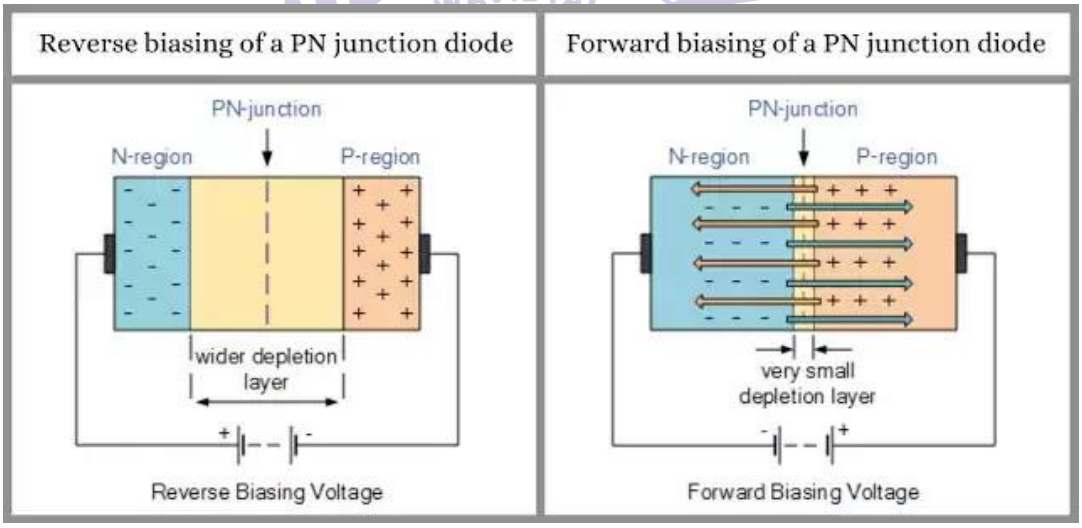


Figure 2. Biasing of PN-Junction diode

ii. **Reverse Biasing-** When N-type (cathode) is connected to + ve terminal and P-type (Anode) is connected to – ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current due to minority charge carriers.

- **CIRCUIT DIAGRAM:-**

(a) **(b)**

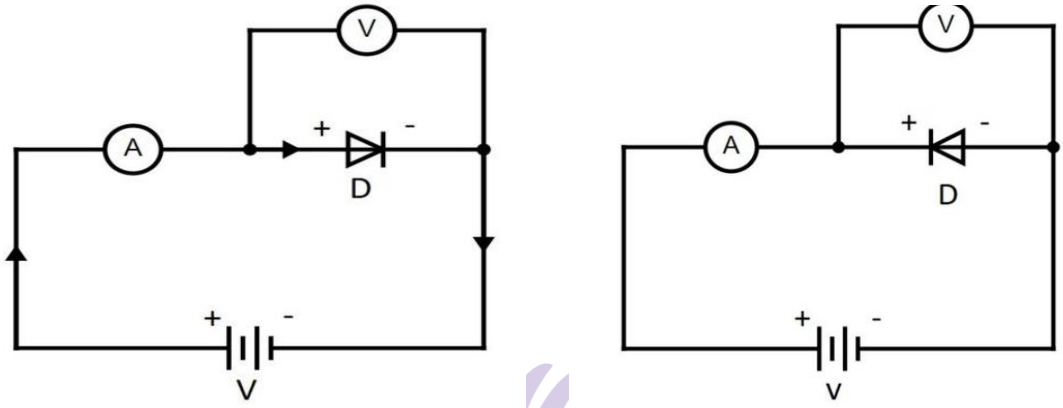


Figure 3.Circuit diagram of (a) Forward and (b) Reverse biasing

- **PROCEDURE:-**

FORWARD BIAS CHARACTERISTICS

1. Make the circuit according to pn junction kit 1V range for voltmeter and 10 mA range for ammeter
    a. By increasing the voltage across the diode in steps of 0.1 volts, note down corresponding current in the table no.1
    b. Calculation of static resistance: Using the forward bias curve, take the points on the Curve beyond the knee voltage and calculate R
2. R static Potential at a point beyond the knee voltage. /Current at that point.

REVERSE BIASED CHARACTERRISTICS

1. Make the circuit according to fig.3 use 10V range for voltmeter and 50 µA range for current meter.
2. By increasing the voltage across the diode in steps of 1.0 volts, note down corresponding current in the table no 2.

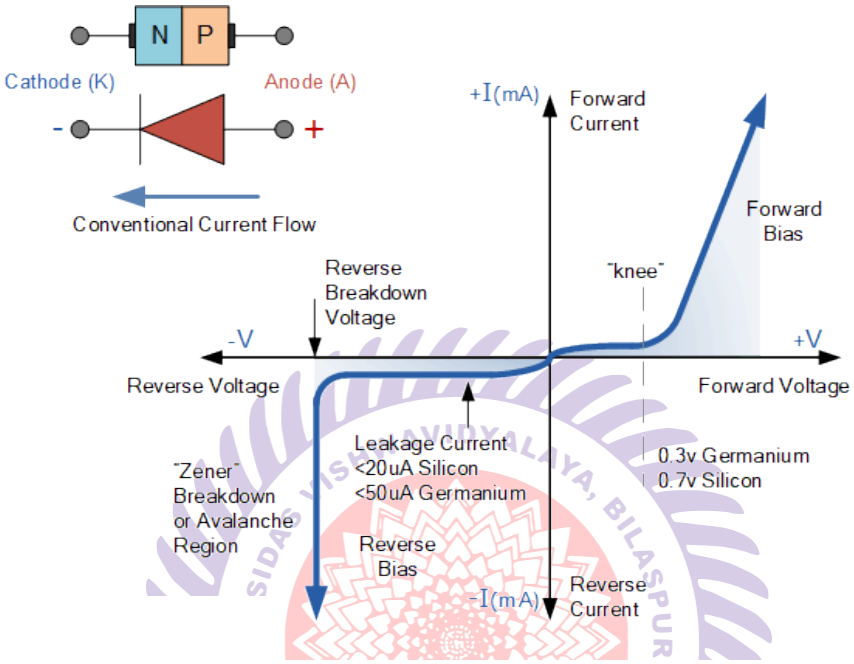
OBSERVATION TABLE-1: FOR FORWARD BIASED

S. No.	Voltage (volts)	Current in (mA)	S. No.	Voltage (volts)	Current in (mA)
1			6		
2			7		
3			8		
4			9		
5			10		

OBSERVATION TABLE-2: FOR REVERSE BIASED

S. No.	Voltage (volts)	Current in (mA)	S. No.	Voltage (volts)	Current in (mA)
1			6		
2			7		
3			8		
4			9		
5			10		

- **RESULT:-** The I/V Characteristic of P-N Junction diode is shown in the graph.



- **PRECAUTIONS:-**

1. Voltmeter and ammeter of appropriate ranges should be selected.
2. The variation in V should be done in steps of 0.1 V.
3. The battery connections of p-n junction diode should be checked and it should be ensured that p is connected to positive and n to the negative of the battery.
4. Never cross the limits specified by the manufacturer otherwise the diode will get damaged.

EXPERIMENT NO. – 02

- **OBJECTIVE:-** To study V-I characteristics of Zener diode and its use as voltage regulator.

- **APPARATUS REQUIRED:-** Semiconductor Zener diode kit and connecting wires.

- **THEORY AND FORMULA USED:-** Zener diode is a P-N junction diode specially designed to operate in the reverse biased mode. It is acting as normal diode while forward biasing. It has a particular voltage known as break down voltage, at which the diode break downs while reverse biased. In the case of normal diodes the diode damages at the break down voltage. But Zener diode is specially designed to operate in the reverse breakdown region.

  The basic principle of Zener diode is the Zener breakdown. When a diode is heavily doped, it's depletion region will be narrow. When a high reverse voltage is applied across the junction, there will be very strong electric field at the junction. And the electron hole pair generation takes place. Thus heavy current flows. This is known as Zener break down. So a Zener diode, in a forward biased condition acts as a normal diode. In reverse biased mode, after the break down of junction current through diode increases sharply. But the voltage across it remains constant.

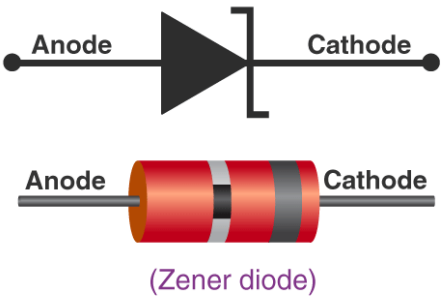


Figure1. Zener diode

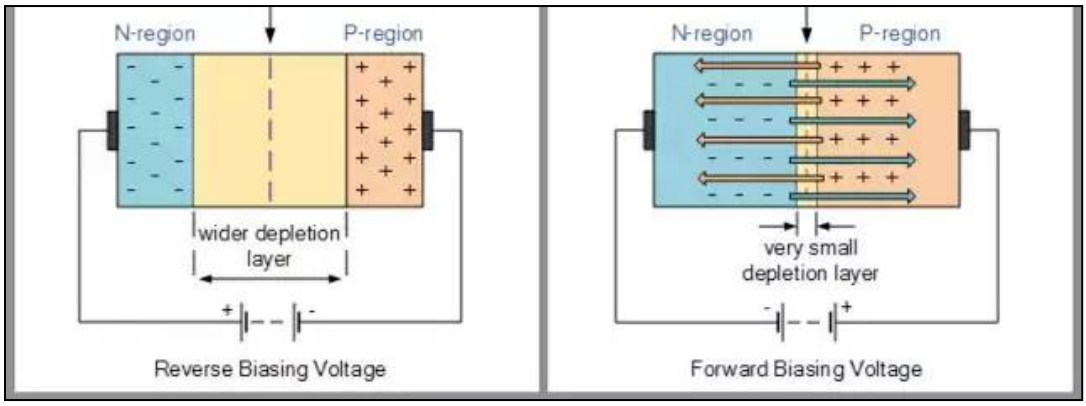


Figure 2. Biasing of Diode

- **Circuit Diagram:-**

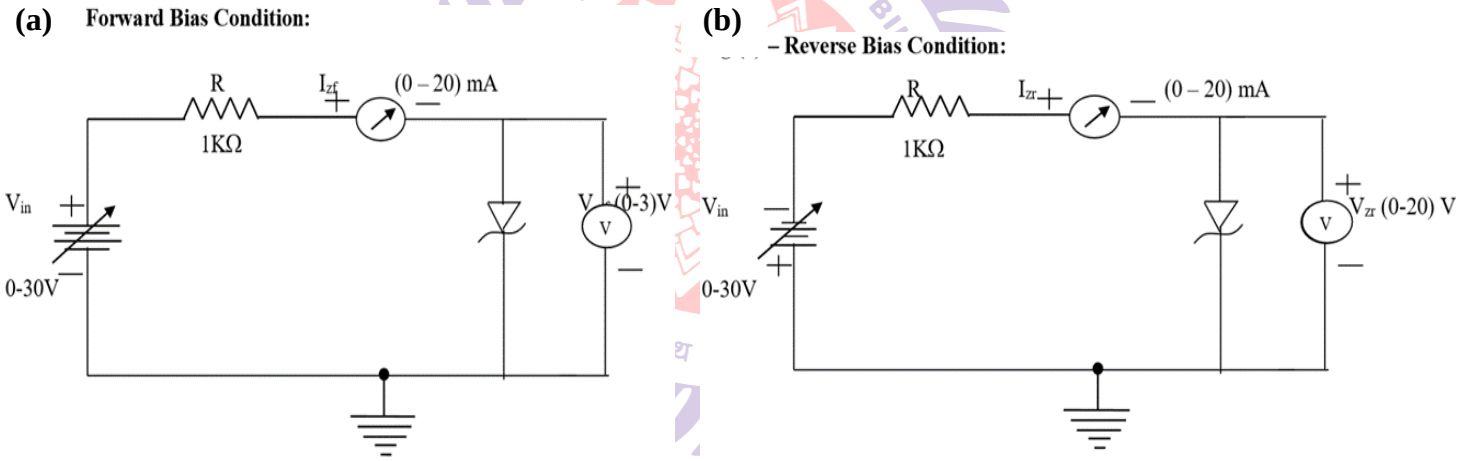


Figure 3.Circuit diagram of (a) Forward and (b) Reverse biasing of Zener Diode

- **PROCEDURE:-**

For zener diode reverse breakdown characteristics of given zener diode

1. Connect the given diode as shown in fig.1a. Identify the voltage polarity meter and diode polarity. Select voltmeter range to 10V. Select mode switch towards V_Z mode.

2. Keep supply control to minimum (fully counter-clockwise). Switch on the power.
3. Gradually increase the supply voltage in small steps and note the readings V_Z, I_Z with each increament till mA meter approaches to maximum.
4. Bring supply control to minimum.Select mode towards V_S. Now again increase the supply and note the input voltage V_S with current I_Z.
5. Plot the reverse bias curve from the observations. Find out the knee of the curve at minimum current.

For zener diode forward breakdown characteristics of given zener diode

1. Connect the given diode as shown in fig.1b. Identify the voltage polarity meter and diode'spolarity. Select voltmeter range to 1V. Select mode switch towards V_Z mode.
2. Keep supply control to minimum (fully counter-clockwise). Switch on the power.
3. Gradually increase the supply voltage in small steps and note the forward breakdown voltage.Increase the supply further and note the current I_{ZF} . Increase further supply till current meter approaches to maximum.
4. Plot the forward bias curve with the reverse bias in 1st quadrent. From the curve it is found that the zener diodes exhibit very low resistance after forward breakdown in forward and reverse bias.

OBSERVATION TABLE-1: FOR FORWARD BIASED

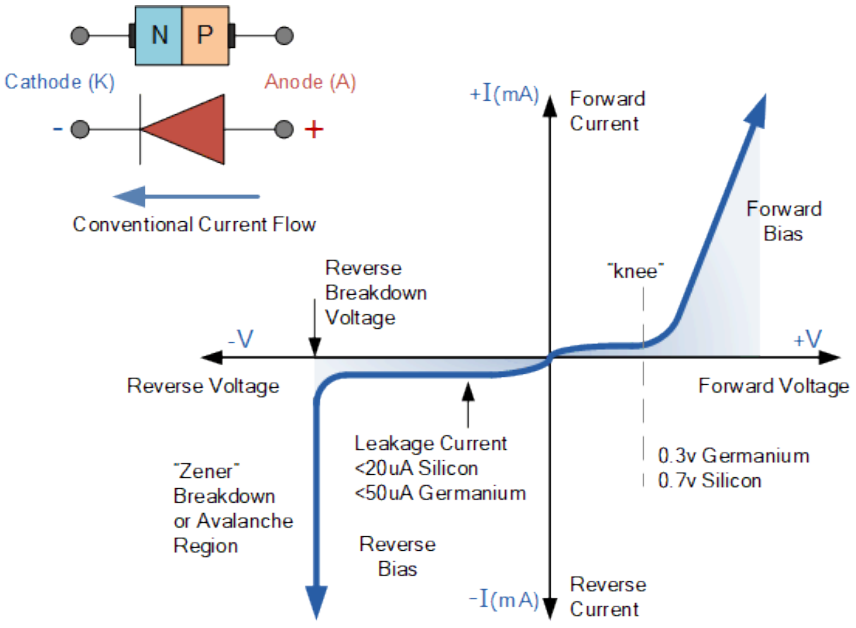
S. No.	Voltage (volts)	Current in (mA)	S. No.	Voltage (volts)	Current in (mA)
1			6		

2			7		
3			8		
4			9		
5			10		

OBSERVATION TABLE-2: FOR REVERSE BIASED

S. No.	Voltage (volts)	Current in (mA)	S. No.	Voltage (volts)	Current in (mA)
1			6		
2			7		
3			8		
4			9		
5			10		

- **RESULT:-** The I/V Characteristic of Zener diode is shown in the graph.



- **PRECAUTIONS:-**

1. Voltmeter and ammeter of appropriate ranges should be selected.
2. The variation in V should be done in steps of 0.1 V.
3. The battery connections of p-n junction diode should be checked and it should be ensured that p is connected to positive and n to the negative of the battery.
4. Never cross the limits specified by the manufacturer otherwise the diode will get damaged.

EXPERIMENT NO. – 03

- **OBJECTIVE:-**To plot the V-I Characteristics of the solar cell and hence determine the fillfactor.

- **APPARATUS REQUIRED:-** Solar cell mounted on the front panel in a metal box with connections brought out on terminals. Two meters mounted on the front panel to measure the solar cell voltage and current. Different types of load resistances selectable using band switch also provided on the front panel. Three single points and two interconnectable patch chords for connections. Wooden plank with half meter scale fitted on it and a lamp holder with 100 watt lamp.

- **THEORY AND FORMULA USED:-** The solar cell is a semi conductor device, which converts the solar energy into electrical energy. It is also called a photovoltaic cell. A solar panel consists of numbers of solar cells connected in series or parallel. The number of solar cell connected in a series generates the desired output voltage and connected in parallel generates the desired output current. The conversion of sunlight(Solar Energy) into electric energy takes place only when the light is falling on the cells of the solar panel. Therefore in most practical applications, the solar panels are used to charge the lead acid or Nickel-Cadmium batteries. In the sunlight, the solar panel charges the battery and also supplies the power to the load directly. When there is no sunlight, the charged battery supplies the required power to the load.

  A solar cell operates in somewhat the same manner as other junction photo detectors. A built-in depletion region is generated in that without an applied reverse bias and photons of adequate

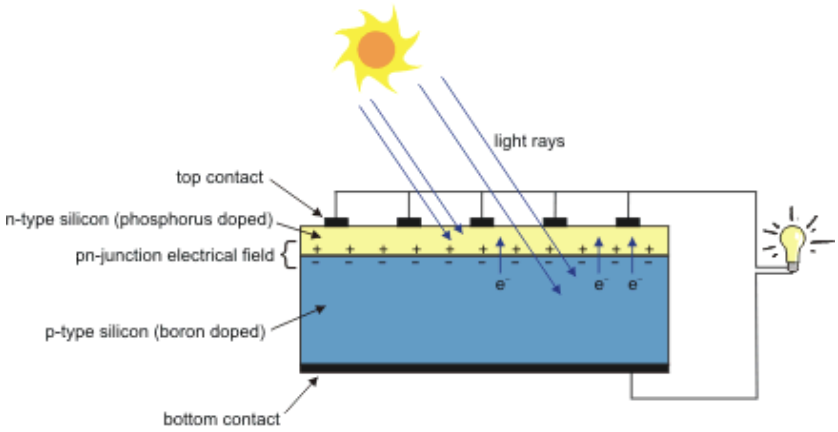


Figure1: Solar Cell

energy create hole-electrons pairs. In the solar cell, as shown in Fig. 1, the pair must diffuse a considerable distance to reach the narrow depletion region to be drawn out as useful current. Hence, there is higher probability of recombination. The current generated by separated pairs increases the depletion region voltage (Photovoltaic effect). When a load is connected across the cell, the potential causes the photocurrent to flow through the load.

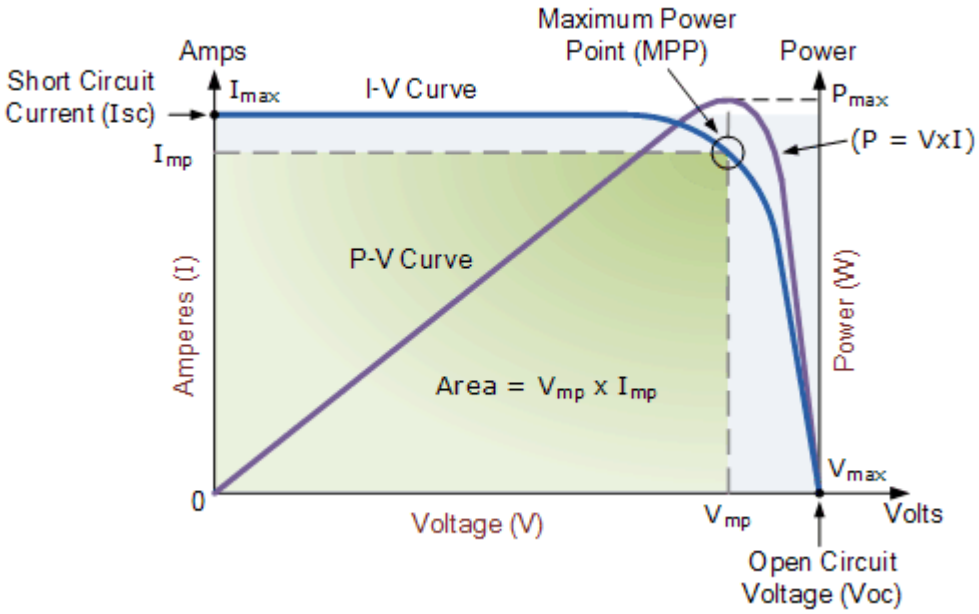


Figure 2: I-V Characteristic of Solar Cells

The e.m.f. generated by the photo-voltaic cell in the open circuit, i.e. when no current is drawn from it is denoted by V_{OC} (V-open circuit). This is the maximum value of e.m.f.. When a high resistance is introduced in the

external circuit a small current flows through it and the voltage decreases. The voltage goes on falling and the current goes on increasing as the resistance in the external circuit is reduced.

When the resistance is reduced to zero the current rises to its maximum value known as saturation current and is denoted as I_{SC}, the voltage becomes zero. A V-I characteristic of a photo- voltaic cell is shown in Fig. 2.

The product of open circuit voltage V_{OC} and short circuit current I_{SC} is known a ideal power.

$$\text{Ideal Power} = V_{OC} \times I_{SC}$$

The maximum useful power is the area of the largest rectangle that can be formed under the V-I curve. If V_m and I_m are the values of voltage and current under this condition, then

$$\text{Maximum useful power} = V_m \times I_m$$

The ratio of the maximum useful power to ideal power is called the fill factor

$$\text{Fill Factor} = \frac{Vm*Im}{Voc*Isc}$$

- **CIRCUIT DIAGRAM:-**

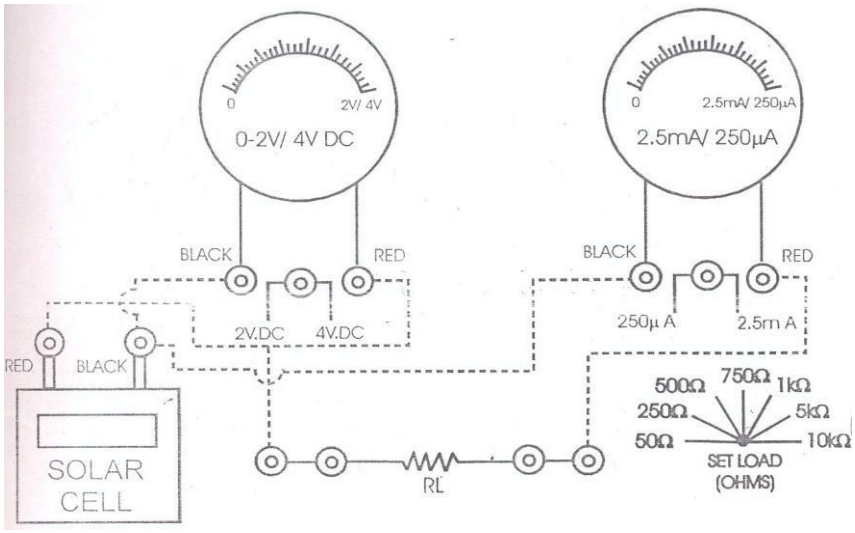


Figure 3. Circuit diagram of Solar cell

- **PROCEDURE:-**

When experiment is performed with 100 Watt lamp:

1. Place the solar cell and the light source (100 watt lamp) opposite to each other on a woodenplank. Connect the circuit as shown by dotted lines (Fig. 3) through patch chords.
2. Select the voltmeter range to 2V, current meter range to 250µA and load resistance (RL) to50Ω.
3. Switch ON the lamp to expose the light on Solar Cell.
4. Set the distance between solar cell and lamp in such a way that current meter shows 250 µAdeflections. Note down the observation of voltage and current in Table 1.
5. Vary the load resistance through band switch and note down the current and voltage readingsevery time in Table 1.
6. Plot a graph between output voltage vs. output current by taking

voltage along X-axis andcurrent along Y-axis.

When experiment is performed in sun light:

1. Connect the circuit as shown by dotted lines (Fig.3) through patch chords.
2. Select the voltmeter range to 4V, current meter range to 2.5mA and load resistance (R_L)to 50Ω.
3. Expose the solar cell to sun light
4. Note down the observation of voltage and current in Table 1.
5. Vary the load resistance through band switch and note down the current and voltagereadings every time in Table 1.
6. Plot a graph between output voltage vs. output current by taking current along X-axis andvoltage along Y-axis. You should get a curve similar to shown in Fig. 2

- **DETERMINING FILL FACTOR**:

Draw a rectangle having maximum area under the V-I curve and note the values of V_m and I_m. Note the voltmeter reading for open circuit, V_{OC} and milliammeter reading with zero resistance I_{SC}. Using these values, calculate the fill factor for the cell.

OBSERVATION TABLE:

Voltmeter reading for open cicuit, V_{OC} = …. Volts

Milliammeter reading with zero resistance, I_{SC} = . . . mA

S. No.	Voltage	Current	Load Resistance (R_L)
1 2 3 4			

5			

- **PRECAUTIONS:**

1. The solar cell should be exposed to sun light before using it in the experiment.
2. Light from the lamp should fall normally on the cell.
3. A resistance in the cell circuit should be introduced so that the current does not exceed thesafe operating limit.

EXPERIMENT NO. – 04

- **OBJECTIVE:-** To study the characteristics of a Bipolar Junction Transistor NPN /PNP in CE configuration.

- **APPARATUS REQUIRED:-** NPN- transistor, Regulated power supply (0-30V), Connecting wires, Resistor, 1KΩ, Voltmeter (0-20V), Ammeters (0-10mA), Bread board (as shown in circuit),

- **THEORY AND FORMULA USED:-** The transistor is a three-layer semiconductor device consisting of either two n- and one p-type layers of material or two p- and one n-type layers of material. The former is called an npn transistor, while the latter is called a pnp transistor. Both are shown in Fig. 1 with the proper dc biasing. The dc biasing is necessary to establish the proper region of operation for ac amplification. The emitter layer is heavily doped, the base lightly doped, and the collector moderately doped. The outer layers have widths much greater than the sandwiched p- or n-type material.

  The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 10:1 or less). These lower doping level decreases the conductivity (increases the resistance) of this material by limiting the number of "free" carriers. For the biasing shown in Fig. 1 the terminals have been indicated by the capital letters E for emitter, C for collector, and B for base. An appreciation for this choice of notation will develop when we discuss the basic operation of the transistor. The abbreviation BJT, from bipolar junction transistor, is often applied to this three terminal device. The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material

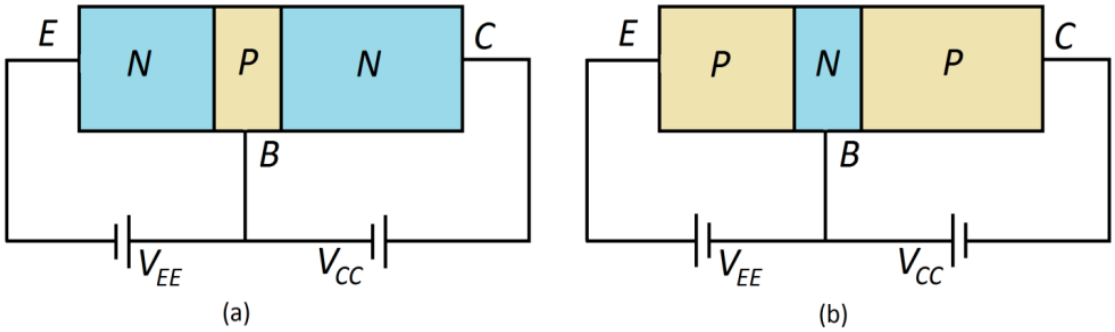


Figure 1. Types of Transistors (a) NPN (b) PNP

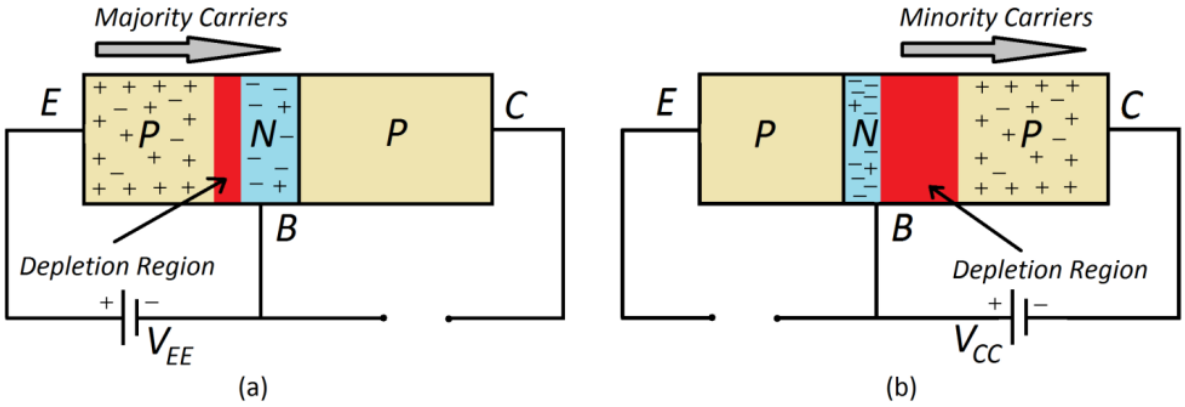


Figure 2. Biasing of a PNP Transistor (a) When collector is open (b) When emitter is open

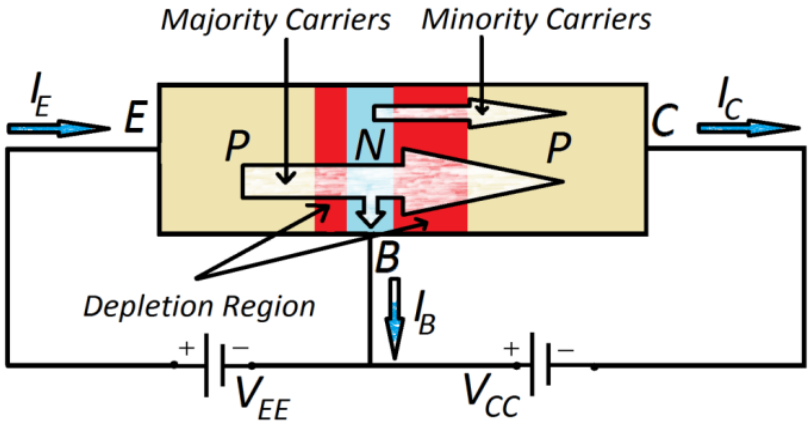


Figure 3. Majority and minority carrier flow of a PNP transistor

- **Circuit Diagram:- Common Emitter configuration of NPN Transistor**

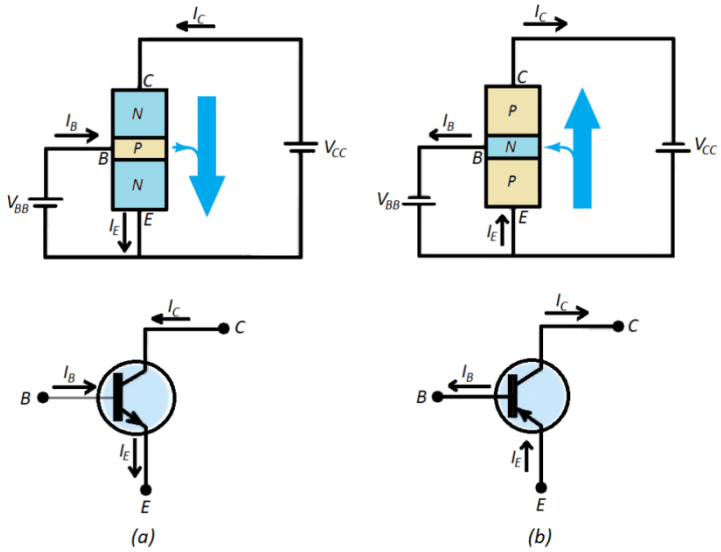


Figure 4. Notations and symbols of common emitter configuration (a) NPN transistor (b) PNP transistor

- **TRANSISTOR OPERATION:-** The basic operation of the transistor will now be described using the pnp transistor as shown in Fig. 2.b. The operation of the npn transistor is exactly the same if the roles played by the electron and hole are interchanged. In Fig. 2.a the pnp transistor has been redrawn without the base-to-collector bias. The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the p- to the n-type material. Let us now remove the base-to-emitter bias of the pnp transistor as shown in Fig. 2.b. The flow of majority carriers is zero, resulting in only a minority-carrier flow, as indicated in Fig. 2.b. Therefore, one p-n junction of a transistor is reverse biased, while the other is forward biased. Applying Kirchhoff's current law to the transistor of Fig. 3 as if it were a single node, we obtain

$$I_E = I_C + I_B \quad (1.1)$$

and find that the emitter current is the sum of the collector and base currents. The collector current, however, is comprised of two components—the majority and minority carriers as indicated in Fig. 3. The minority current

component is called the *leakage current* and is given the symbol I_{CO} (*IC* current with emitter terminal Open). The collector current, therefore, is determined in total by Eq. (1.2).

$$I_C = I_{C\text{majority}} + I_{CO\text{minority}} \quad (1.2)$$

For general-purpose transistors, *IC* is measured in milliamperes, while I_{CO} is measured in microamperes or nanoamperes. I_{CO}, like *Is* for a reverse-biased diode, is temperature sensitive and must be examined carefully when applications of wide temperature ranges are considered. It can severely affect the stability of a system at high temperature if not considered properly. Improvements in construction techniques have resulted in significantly lower levels of I_{CO}, to the point where its effect can often be ignored.

- **Common Emitter Configuration:-** The most frequently encountered transistor configuration appears in Fig. 6 for the *pnp* and *npn* transistors. It is called the *common-emitter configuration* since the emitter is common or reference to both the input and output terminals (in this case common to both the base and collector terminals). Two sets of characteristics are again necessary to describe fully the behavior of the common-emitter configuration: one for the *input* or *base-emitter* circuit and one for the *output* or *collector-emitter* circuit. Both are shown in Fig. 2(a) and (b).

  The emitter, collector, and base currents are shown in their actual conventional current direction. Even though the transistor configuration has changed, the current relations developed earlier for the common-base configuration are still applicable. That is,

  $$I_E = I_C + I_B$$

  and $I_C = \alpha I_E$. For the common-emitter configuration the output characteristics are a plot of the output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B). The input

characteristics are a plot of the input current (I_B) versus the input voltage (V_{BE}) for a range of values of output voltage (V_{CE}).

Note that on the characteristics of Fig. 5 the magnitude of I_B is in microamperes, compared to milliamperes of I_C. Consider also that the curves of I_B are not as horizontal as those obtained for I_E in the common- base configuration, indicating that the collector-to-emitter voltage will influence the magnitude of the collector current.

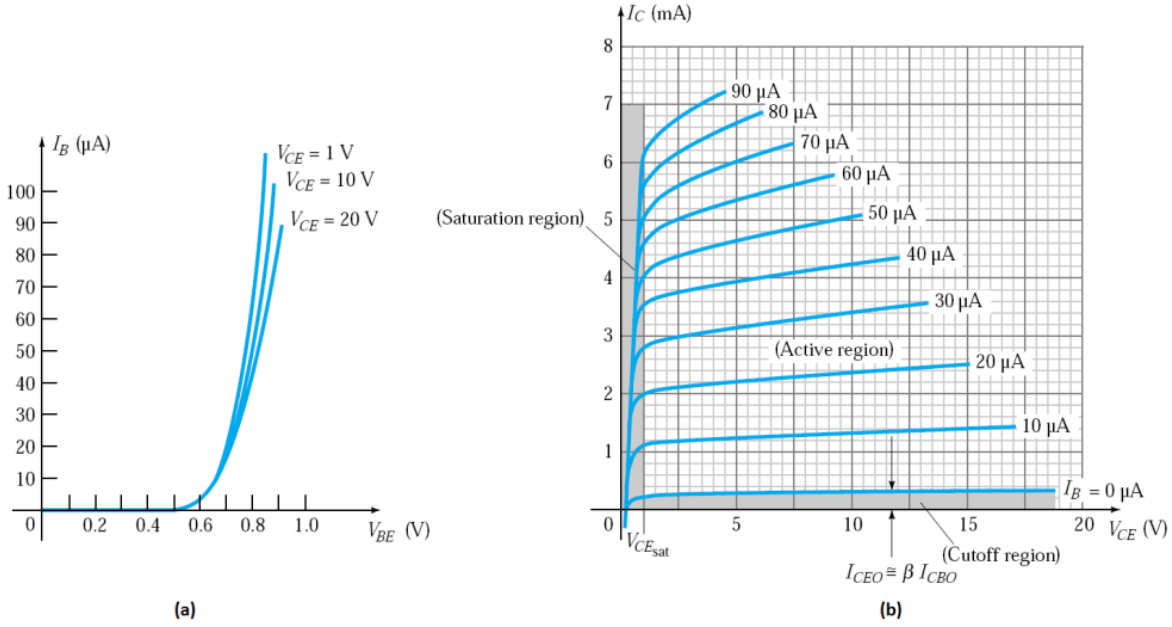


Figure 5. Characteristics for a common emitter configuration (a) Input characteristics, (a) Output characteristics

The active region for the common-emitter configuration is that portion of the upper-right quadrant that has the greatest linearity, that is, that region in which the curves for *IB* are nearly straight and equally spaced. In Fig. 5(b) this region exists to the right of the vertical dashed line at $V_{CE\text{sat}}$ and above the curve for I_B equal to zero. The region to the left of $V_{CE\text{sat}}$ is called the saturation region. ***In the active region of a common-emitter amplifier the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.***

You will recall that these were the same conditions that existed in the active region of the common-base configuration. The active region of the common-emitter configuration can be employed for

voltage, current, or power amplification.

- **PROCEDURE:-**

(A) INPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. For plotting the input characteristics, the output voltage V_{CE} is kept constant at 0V and for different values of V_{EE} , note down the values of I_E and V_{BE}.
3. Repeat the above step keeping V_{CB} at 2V, 4V, and 6V and all the readings are tabulated.
4. A graph is drawn between V_{EB} and I_E for constant V_{CB}.

(B) OUTPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. For plotting the output characteristics, the input I_E is kept constant at 0.5mA and for different values of V_{CC}, note down the values of IC and V_{CB}.
3. Repeat the above step for the values of I_E at 1mA, 5mA and all the readings are tabulated.
4. A graph is drawn between V_{CB} and Ic for constant I_E.

OBSERVATION TABLE:

(A) INPUT CHARACTERISTICS:

V_{EE}(V)	V_{CB}=1V		V_{CB}=2V		V_{CB}=4V	
	V_{EB}(V)	**I_E(mA)**	**V_{EB}(V)**	**I_E(mA**	**V_{EB}(V**	**I_E(mA**

(B) OUTPUT CHARACTERISTICS:

V_{cc}(V)	I_E=10mA		I_E=20mA		I_E=30mA	
	V_{CB}(V	**I_C(mA**	**V_{CB}(V**	**I_C(mA**	**V_{CB}(V**	**I_C(mA**

- **PRECAUTIONS:**

  1. The supply voltages should not exceed the rating of the transistor.
  2. Meters should be connected properly according to their polarities.

- **RESULT:** The Current gain of the Transistor in CB is _____ , the input Resistance is _____ and the output Resistance is _____.

EXPERIMENT NO. – 05

- **OBJECTIVE:-** To study the characteristics of a Bipolar Junction Transistor NPN /PNP in CE configuration.

- **APPARATUS REQUIRED:-** NPN- transistor, Regulated power supply (0-30V), Connecting wires, Resistor, 1KΩ, Voltmeter (0-20V), Ammeters (0-10mA), Bread board (as shown in circuit),

- **THEORY AND FORMULA USED:-** The transistor is a three-layer semiconductor device consisting of either two n- and one p-type layers of material or two p- and one n-type layers of material. The former is called an npn transistor, while the latter is called a pnp transistor. Both are shown in Fig. 1 with the proper dc biasing. The dc biasing is necessary to establish the proper region of operation for ac amplification. The emitter layer is heavily doped, the base lightly doped, and the collector moderately doped. The outer layers have widths much greater than the sandwiched p- or n-type material.

  The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 10:1 or less). These lower doping level decreases the conductivity (increases the resistance) of this material by limiting the number of "free" carriers. For the biasing shown in Fig. 1 the terminals have been indicated by the capital letters E for emitter, C for collector, and B for base. An appreciation for this choice of notation will develop when we discuss the basic operation of the transistor. The abbreviation BJT, from bipolar junction transistor, is often applied to this three terminal device. The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material

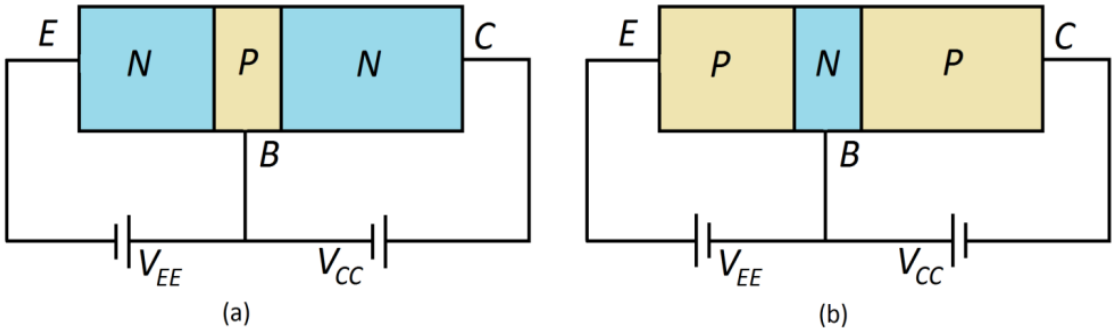


Figure 1. Types of Transistors (a) NPN (b) PNP

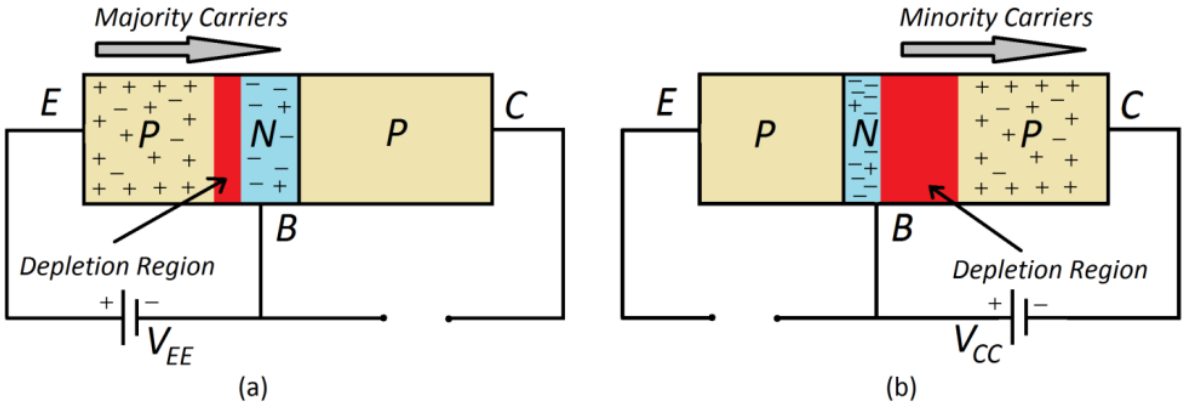


Figure 2. Biasing of a PNP Transistor (a) When collector is open (b) When emitter is open

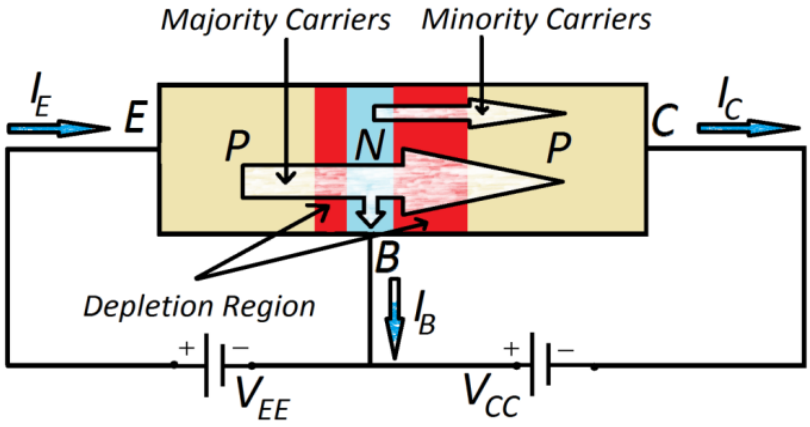


Figure 3. Majority and minority carrier flow of a PNP transistor

- **Circuit Diagram:- Common Emitter configuration of NPN Transistor**

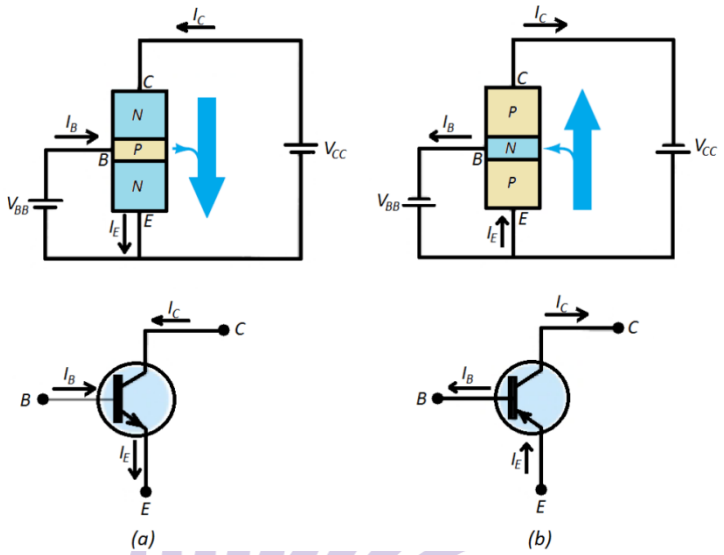


Figure 4. Notations and symbols of common emitter configuration (a) NPN transistor (b) PNP transistor

- **TRANSISTOR OPERATION:-** The basic operation of the transistor will now be described using the pnp transistor as shown in Fig. 2.b. The operation of the npn transistor is exactly the same if the roles played by the electron and hole are interchanged. In Fig. 2.a the pnp transistor has been redrawn without the base-to-collector bias. The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the p- to the n-type material. Let us now remove the base-to-emitter bias of the pnp transistor as shown in Fig. 2.b. The flow of majority carriers is zero, resulting in only a minority-carrier flow, as indicated in Fig. 2.b. Therefore, one p-n junction of a transistor is reverse biased, while the other is forward biased. Applying Kirchhoff's current law to the transistor of Fig. 3 as if it were a single node, we obtain

$$I_E = I_C + I_B \quad (1.1)$$

and find that the emitter current is the sum of the collector and base currents. The collector current, however, is comprised of two components—the majority and minority carriers as indicated in Fig. 3. The minority current component is called the *leakage current* and is given the symbol I_{CO} (*IC* current with emitter terminal Open). The collector current, therefore, is determined in total by Eq. (1.2).

$$I_C = I_{C\text{majority}} + I_{CO\text{minority}} \quad (1.2)$$

For general-purpose transistors, *IC* is measured in milliamperes, while I_{CO} is measured in microamperes or nanoamperes. I_{CO}, like *Is* for a reverse-biased diode, is temperature sensitive and must be examined carefully when applications of wide temperature ranges are considered. It can severely affect the stability of a system at high temperature if not considered properly. Improvements in construction techniques have resulted in significantly lower levels of I_{CO}, to the point where its effect can often be ignored.

- **Common Emitter Configuration:-** The most frequently encountered transistor configuration appears in Fig. 6 for the *pnp* and *npn* transistors. It is called the *common-emitter configuration* since the emitter is common or reference to both the input and output terminals (in this case common to both the base and collector terminals). Two sets of characteristics are again necessary to describe fully the behavior of the common-emitter configuration: one for the *input* or *base-emitter* circuit and one for the *output* or *collector-emitter* circuit. Both are shown in Fig. 2(a) and (b).

  The emitter, collector, and base currents are shown in their actual conventional current direction. Even though the transistor configuration has changed, the current relations developed earlier for the common-base configuration are still applicable. That is,

$$I_E = I_C + I_B$$

and $I_C = \alpha I_E$. For the common-emitter configuration the output characteristics are a plot of the output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B). The input characteristics are a plot of the input current (I_B) versus the input voltage (V_{BE}) for a range of values of output voltage (V_{CE}).

Note that on the characteristics of Fig. 5 the magnitude of I_B is in microamperes, compared to milliamperes of I_C. Consider also that the curves of I_B are not as horizontal as those obtained for I_E in the common- base configuration, indicating that the collector-to-emitter voltage will influence the magnitude of the collector current.

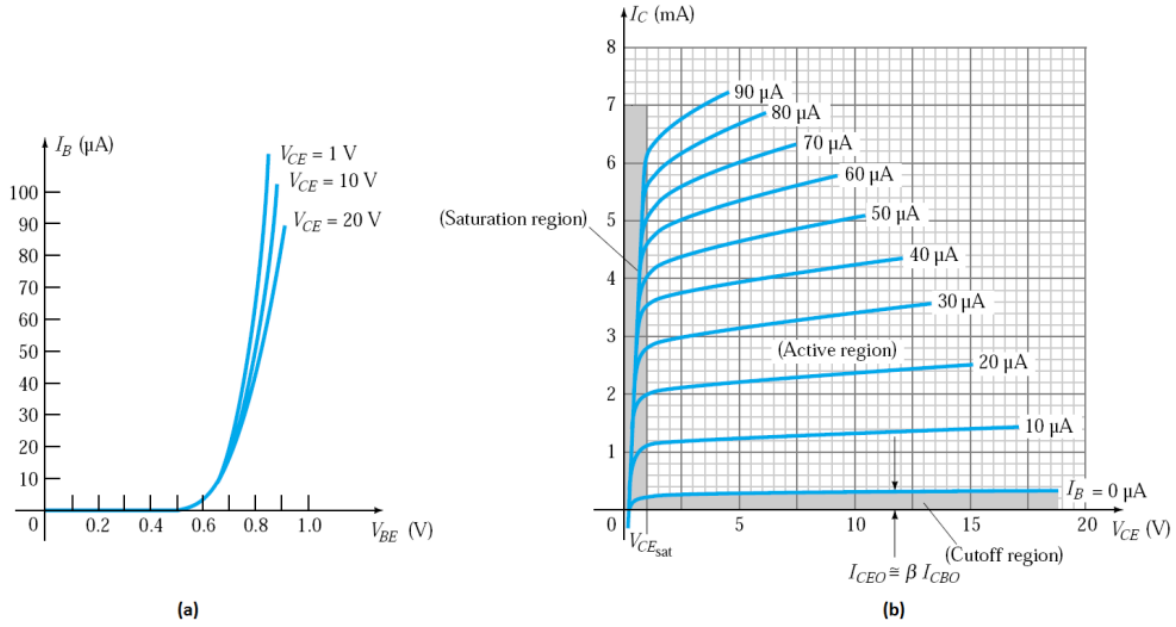


Figure 5. Characteristics for a common emitter configuration (a) Input characteristics, (a) Output characteristics

The active region for the common-emitter configuration is that portion of the upper-right quadrant that has the greatest linearity, that is, that region in which the curves for *IB* are nearly straight and equally spaced. In Fig. 5(b) this region exists to the right of the vertical dashed line at $V_{CE\text{sat}}$ and above the curve for I_B equal to zero. The region to the left of $V_{CE\text{sat}}$ is called the saturation region. ***In the active region of a common-emitter amplifier the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.***

You will recall that these were the same conditions that existed in the active region of the common-base configuration. The active region of the common-emitter configuration can be employed for voltage, current, or power amplification.

- **PROCEDURE:-**

(A) INPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. For plotting the input characteristics, the output voltage V_{CE} is kept constant at 0V and for different values of V_{EE} , note down the values of I_E and V_{BE}
3. Repeat the above step keeping V_{CB} at 2V, 4V, and 6V and all the readings are tabulated.
4. A graph is drawn between V_{EB} and I_E for constant V_{CB}.

(B) OUTPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. For plotting the output characteristics, the input I_E is kept constant at 0.5mA and for different values of V_{CC}, note down the values of IC and V_{CB}.
3. Repeat the above step for the values of I_E at 1mA, 5mA and all the readings are tabulated.
4. A graph is drawn between V_{CB} and Ic for constant I_E.

OBSERVATION TABLE:

(A) INPUT CHARACTERISTICS:

V_{EE}(V)	V_{CB}=1V		V_{CB}=2V		V_{CB}=4V	
	V_{EB}(V)	**I_E(mA)**	**V_{EB}(V)**	**I_E(mA**	**V_{EB}(V**	**I_E(mA**

(B) OUTPUT CHARACTERISTICS:

V_{cc}(V)	I_E=10mA		I_E=20mA		I_E=30mA	
	V_{CB}(V	**I_C(mA**	**V_{CB}(V**	**I_C(mA**	**V_{CB}(V**	**I_C(mA**

- **PRECAUTIONS:**

1. The supply voltages should not exceed the rating of the transistor.
2. Meters should be connected properly according to their polarities.

- **RESULT:** The Current gain of the Transistor in CB is _____ , the input Resistance is _____ and the output Resistance is _____.

EXPERIMENT NO. – 06

- **OBJECTIVE:-** To study the Colpitt's oscillator

- **APPARATUS REQUIRED:-** n-p-n transistor, Carbon resistors (as shown in circuit), inductor, capacitors, dc power supply, CRO and connecting terminals.

- **THEORY AND FORMULA USED:-** When the collector supply voltage V_{cc} is switched on, collector current starts rising and charges the capacitors C_1 and C_2. When these capacitors are fully charged, they discharge through coil L setting up damped harmonic oscillations in the tank circuit. The oscillatory current in the tank circuit produces an a.c. voltages across C_1, C_2. The oscillations across C_2 are applied to base-emitter junction of the transistor and appears in the amplified form in the collector circuit and overcomes the losses occurring in the tank circuit.

  The feedback voltage (across the capacitor C_2) is 180° out of phase with the output voltage(across the capacitor C_1), as the centre of the two capacitors is grounded. A phase shift of 180° is produced by the feedback network and a further phase shift of 180° between the output and input voltage is produced by the CE transistor. Hence, the total phase shift is 360° or 0°, which is essential for sustained oscillations, as per, the Barkhausen criterion. So we get continuous undamped oscillations.

  The frequency of oscillation of the oscillator $f = \frac{1}{2\pi\sqrt{LC}}\ Hz$

  Where, L = Self inductance of the coil (H) , C = Capacitance of the condenser (F)

  $C = \frac{C1*C2}{C1+C2}$ = Resultant capacitance of the series combination

Where C_1, C_2 = capacitances of the two capacitors in the tank circuit.

- **CIRCUIT DIAGRAM:-** The circuit diagram of Colpitt's oscillator using BJT is shown in Fig. It consists of an R-C coupled amplifier using an n-p-n transistor in CE configuration. R_1 and R_2 are two resistors which form a voltage divider bias to the transistor. A resistor R_E is connected in the circuit which stabilizes the circuit against temperature variations. A capacitor C_E is connected in parallel with R_E, acts as a bypass capacitor and provides a low reactive path to the amplified ac signal. The coupling capacitor C_C blocks dc and provides an ac path from the collector to the tank circuit. The feedback network (tank circuit) consists of two capacitors C_1 and C_2 (in series) which placed across a common inductor L. The centre of the two capacitors is tapped (grounded). The feedback network (C_1, C_2 and L) determines the frequency of oscillation of the oscillator. The two series capacitors C_1, and C_2 form the potential divider led for providing the feedback voltage. The voltage developed across the capacitor C_2 provides regenera tive feedback which is essential for sustained oscillations.

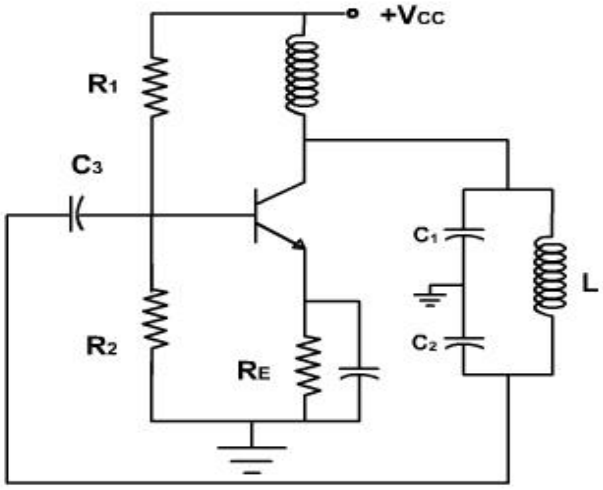


Figure 1: Circuit Diagram of Colpitt's Oscillator

- **PROCEDURE:-** The circuit is connected as shown in figure. Connect the CRO across the output terminals of the oscillator. Switch on the power supply to both the oscillator and CRO. Select proper values of L, C_1 and C_2 in the oscillator circuit and get the sine wave form on the screen of CRO. The voltage (deflection) sensitivity band switch (Y-plates) and time base band switch (X-plates) are adjusted such that a steady and complete picture of one or two sine waveform is obtained on the screen. The horizontal length (l) between two successive peaks is noted. When this horizontal length (l), is multiplied by the time base (m) i.e. sec/div , we get the time-period (T = l x m).The reciprocal of the time-period(1/T) gives the frequency(f). This can be verified with the frequency, calculated theoretically by using the above formula. The experiment is repeated by changing L or C_1 or C_2 or all. The readings are noted in the table given.

OBSERVATION TABLE

S.No	Inductance (mH)	Capacitance (μF)			Measurement of time period			Frequency (Hz)	
	L	C_1	C_2	$C = \frac{C_1 C_2}{C_1 + C_2}$	Peak to peak (Horizontal) length (Div) (l)	Time-base Sec/Div (m)	Time-period T = mxl Sec.	Expt. $f = \frac{1}{T}$	Theoritical $f = \frac{1}{2\pi\sqrt{LC}}$

- **PRECAUTIONS:-**

1. Check the continuity of the connecting terminals before going to connect the circuit.
2. Identify the emitter, base and collector of the transistor properly before connecting it inthe circuit.
3. The horizontal length between two successive peaks should accurately be measured.

EXPERIMENT NO. – 07

- **OBJECTIVE:-** To study the Hartley's oscillator

- **APPARATUS REQUIRED:-** n-p-n transistor, Carbon resistors (as shown in circuit), inductor, capacitors, dc power supply, CRO and connecting terminals.

- **THEORY AND FORMULA USED:-**When the collector supply voltage Vcc is switched on, collector current starts rising and charges the capacitor C. When this capacitor is fully charged, it discharges through coils L1 and L2, setting up damped harmonic oscillations in the tank circuit. The oscillatory current in the tank circuit produces an a.c. voltage across L1 which *is* applied to the base emitter junction of the transistor and appears in the amplified form in the collector circuit. Feedback of energy from output (collector emitter circuit) to input (base-emitter circuit is) accomplished through auto transformer action. The output of the amplifier is applied across the inductor L1, and the voltage across L2 forms the feedback voltage. The coil L1, is inductively coupled to coil L2, and the combination acts as an auto-transformer. This energy supplied to the tank circuit overcomes the losses occurring in it. Consequently the oscillations are sustained in the circuit.

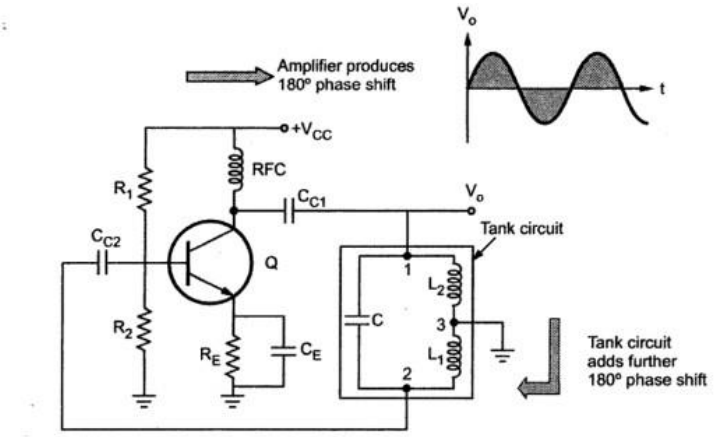
  The energy supplied to the tank circuit is in phase with the generated oscillations. The phase difference between the voltages across L1 and that across L2 is always 180° because the centre of the two is grounded. A further phase of 180° is introduced between the input and output voltages by the transistor itself. Thus the total phase shift becomes 3600 (or zero), thereby making the feedback positive or

regenerative which is essential for oscillations. So continuous undamped oscillations are obtained.

The frequency of oscillation of the oscillator $f = \frac{1}{2\pi\sqrt{LC}}\ Hz$

Where L = L1+L2 = series combination of inductance and C is capacitance.

- **CIRCUIT DIAGRAM:-** The circuit diagram of Hartley oscillator (parallel or shunt-fed) using BJT is shown in Figure. It consists of an R-C coupled amplifier using an n-p-n transistor in CE configuration. R1 and R2 are two resistors which form a voltage divider bias to the transistor. A resistor RE is connected in the circuit which stabilizes the circuit against temperature variations. A capacitor CE is connected in parallel with RE, acts as a bypass capacitor and provides a low reactive path to the amplified ac signal. The coupling capacitor CC blocks dc and provides an ac path from the collector to the tank circuit. The L-C feedback network (tank circuit) consists of two inductors L1, and L2 (in series) which are placed across a common capacitor C and the centre of the two inductors is tapped as shown in fig. The feedback network (L1, L2 and C) determines the frequency of oscillation of the oscillator.



- **PROCEDURE:-** The circuit is connected as shown in figure. Connect the CRO across the output terminals of the oscillator. Switch on the power supply to both the oscillator and CRO. Select proper values of C, L1 and L2 in the oscillator circuit and get the sine wave form on the screen of CRO. The voltage (deflection) sensitivity band switch (Y-plates) and time base band switch (X-plates) are adjusted such that a steady and complete picture of one or two sine waveform is obtained on the screen. The horizontal length (l) between two successive peaks is noted. When this horizontal length (l), is multiplied by the time base (m) i.e. sec/div , we get the time-period (T = l x m).The reciprocal of the time-period(1/T) gives the frequency (f). This can be verified with the frequency, calculated theoretically by using the above formula. The experiment is repeated by changing C or L1 or L2 or all. The readings are noted in the table given.

OBSERVATION TABLE

S No	Capacitance (μF)	Inductance (mH)			Measurement of time period			Frequency (Hz)	
	C	L_1	L_2	$L = L_1 + L_2$	Peak to peak (Horizontal) length (Div) (l)	Time-base Sec/Div (m)	Time-period T = mxl Sec.	$f = \frac{1}{T}$	$f = \frac{1}{2\pi\sqrt{LC}}$

- **PRECAUTIONS:-**

4. Check the continuity of the connecting terminals before going to connect the circuit.
5. Identify the emitter, base and collector of the transistor properly before connecting it inthe circuit.
6. The horizontal length between two successive peaks should accurately be measured.