LAB MANUAL

EC206PPC09

Electronic Devices Lab

Bachelor of Technology

in

Electronics & Communication Engineering

Department of Electronics & Communication Engineering

School of Studies of Engineering & Technology

Guru Ghasidas Vishwavidyalaya

Bilaspur-495009 (C. G.)

Website: www.ggu.ac.in

SCHOOLOFSTUDIESOFENGINEERING&TECHNOLOGY
GURU GHASIDAS VISHWAVIDYALAYA, BILASPUR (C.G.)
(ACENTRALUNIVERSITY)
NEP SYLLABUS
B. TECH. SECOND YEAR(ElectronicsandCommunicationEngineering)
(W.E.F.SESSION2021-22)

Vision and Mission of the Institute

Vision		To be a leading technological institute that imparts transformative education to create globally competent technologists, entrepreneurs, researchers and leaders for a sustainable society
Mission	1	To create an ambience of teaching learning through transformative education for future leaders with professional skills, ethics, and conduct.
	2	To identify and develop sustainable research solutions for the local and global needs.
	3	To build a bridge between the academia, industry and society to promote entrepreneurial skills and spirit

Vision and Mission of the Department

Vision		The Department endeavours for academic excellence in Electronics & Communication Engineering by imparting in depth knowledge to the students, facilitating research activities and cater to the ever-changing industrial demands, global and societal needs with leadership qualities.
Mission	1	To be the epitome of academic rigour, flexible to accommodate every student and faculty for basic, current and future technologies in Electronics and Communication Engineering with professional ethics.
	2	To develop an advanced research centre for local & global needs.
	3	To mitigate the gap between academia, industry & societal needs through entrepreneurial and leadership promotion.

Program Educational Objectives (PEOs)

The graduate of the Electronics and Communication Engineering Program will

PEO1: Have fundamental and progressive knowledge along with research initiatives in the field of Electronics & Communication Engineering.

PEO2: Be capable to contrive solutions for electronic & communication systems for real world applications which are technically achievable and economically feasible leading to academia, industry, government and social benefits.

PEO3: Have performed effectively in a multi-disciplinary environment and have self-learning & self-perceptive skills for higher studies, professional career or entrepreneurial endeavors to be confronted with a number of difficulties.

1

PEO4: Attain team spirit, communication skills, ethical and professional attitude for lifelong learning.

ProgrammeOutcomes: Graduateswillbe ableto:

PO1:Fundamentals: Applyknowledgeofmathematics,scienceandengineering.

PO2:Problemanalysis:Identify,formulateandsolverealtimeengineeringproblemsusingfirstprinciples.

PO3:Design: Designengineeringsystemscomplyingwithpublichealth,safety,cultural,societalandenvironmentalconsiderations

PO4:Investigation: Investigatecomplexproblemsbyanalysisandinterpretingthedatatosynthesize validsolution.

PO5:Tools: Predictandmodelbyusingcreativetechniques,skillsandITtoolsnecessaryformodernengineeringpractice.

PO6:Society: Applytheknowledgetoassesssocietal,health,safety,legalandculturalissuesforpracticingengineeringprofession.

PO7: Environment: Understand the importance of the environment for sustainable development.

PO8:Ethics: Applyethicalprinciplesandcommittoprofessionalethics,andresponsibilitiesandnormsof theengineering practice.

PO9:Teamwork: Functioneffectivelyasanindividualandasamemberorleaderindiverseteamsandmultidisciplinary settings.

PO10:Communication: Communicateeffectivelybypresentationsandwritingreports.

PO11:Management: Manageprojectsinmultidisciplinaryenvironmentsasmemberorateamleader.

PO12:Life-longlearning: Engageinindependentlifelonglearninginthebroadestcontextoftechnologicalchange.

ProgrammeSpecificOutcomes:

PSO1: Identify, formulateand applyconcepts acquired through Electronics&CommunicationEngineeringcoursestothereal-world applications.

PSO2: Designandimplementproductsusingthecutting-edgesoftwareandhardwaretoolstoattainskillsforanalyzinganddevelopingsubsystem/processes.

PSO3: Abilitytoadaptandcomprehendthetechnologyadvancementinresearchandcontemporaryindustry demands with demonstration of leadership qualities and betterment of organization,environment andsociety.

Sub Code	L	T	P	Duration	IA	ESE	Total	Credits
EC205THS03	-	–	3	3 hours	30	70	100	3

ELECTRONIC DEVICES LAB

Course Objectives:

- To identify and test various electronic components.
- To use CRO/DSO & function generator for various measurements.
- To plot the characteristics of diode and transistor.
- To observe the waveform of rectifiers & filters.

2

Course Outcomes:

At the end of the course, students will be able to:

    CO1 Illustrate the characteristics of diode.

    CO2 Implement rectifier circuits and evaluate the efficiency.

    CO3 Implement the filter circuits and analyze the practical applications for filters.

    CO4 Implement the different configuration of BJT and analyze their characteristics.

    CO5 Design JFET & MOSFET and analyze their characteristics.

CourseOutcomesandtheirmappingwithProgramOutcomes & Program Specific Outcomes:

CO	PO												PSO		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	1	1	1	1			2			3	2	2	1
CO2	3	2	1	1	1	1			2			3	2	2	1
CO3	3	2	1	1	1	1			2			3	2	2	1
CO4	3	2	1	1	1	1			2			3	2	2	1
CO5	3		2	1	1	1	1			2			3	2	2	1

Weightage: **1–Sightly; 2–Moderately; 3–Strongly**

<center># EXPERIMENT-1</center>

Objective: To verify V-I characteristics of the PN junction diode.

Apparatus required

Power supply

Lab trainer kit

Jumper wires

Multimeter

Theory

Structure of P-N junction diode

The diode is a device formed from a junction of n-type and p-type semiconductor material. The lead connected to the p-type material is called the anode and the lead connected to the n-type material is the cathode. In general, the cathode of a diode is marked by a solid line on the diode.
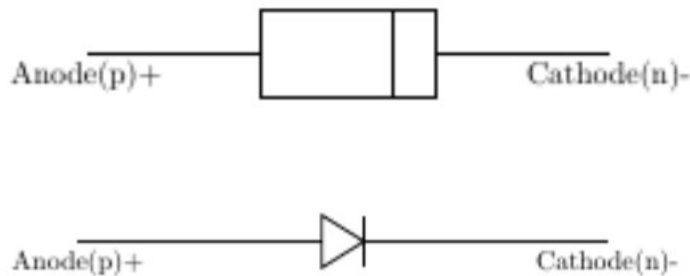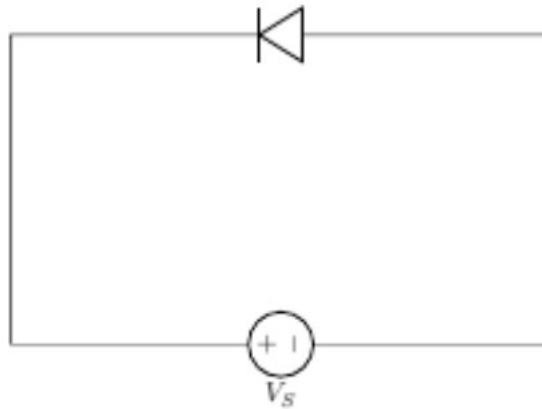

Function of a P-N junction diode in Forward Bias

The positive terminal of battery is connected to the P side(anode) and the negative terminal of battery is connected to the N side(cathode) of a diode, the holes in the p-type region and the electrons in the n-type region are pushed toward the junction and start to neutralize the depletion zone, reducing its width. The positive potential applied to the p-type material repels the holes, while the negative potential applied to the n-type material repels the electrons. The change in potential between the p side and the n side decreases or switches sign. With increasing forward-bias voltage, the depletion zone eventually becomes thin enough that the zone's electric field cannot counteract charge carrier motion across the p–n junction, which as a consequence reduces electrical resistance. The electrons that cross the p–n junction into the p-type material (or holes that cross into the n-type material) will diffuse into the nearby neutral region. The amount of minority diffusion in the near-neutral zones determines the amount of current that may flow through the diode.
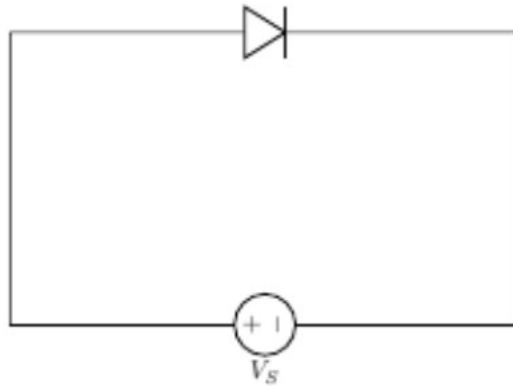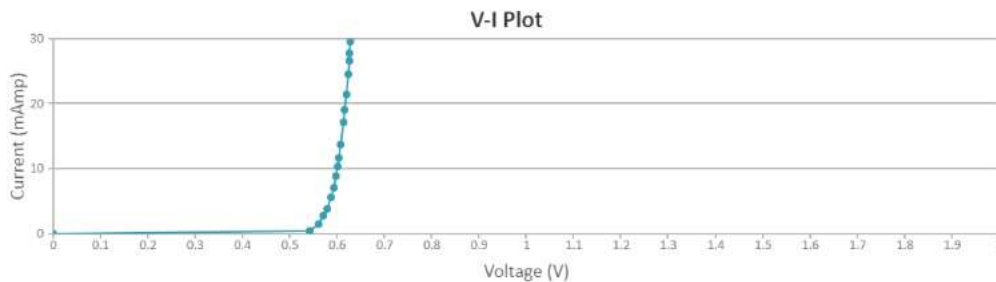
Function of a P-N junction diode in Reverse Bias

The positive terminal of the battery is connected to the N side(cathode) and the negative terminal of the battery is connected to the P side(anode) of a diode. Therefore, very little current will flow until the diode breaks down.

The positive terminal of battery is connected to the N side(cathode) and the negative terminal of battery is connected to the P side(anode) of a diode, the 'holes' in the p-type material are pulled away from the junction, leaving behind charged ions and causing the width of the depletion region to increase. Likewise, because the n-type region is connected to the positive terminal, the electrons will also be pulled away from the junction, with similar effect. This increases the voltage barrier causing a high resistance to the flow of charge carriers, thus allowing minimal electric current to cross the p–n junction. The increase in resistance of the p–n junction results in the junction behaving as an insulator. The strength of the depletion zone electric field increases as the reverse-bias voltage increases. Once the electric field intensity increases beyond a critical level, the p–n junction depletion zone breaks down and current begins to flow, usually by either the Zener or the avalanche breakdown processes. Both of these breakdown processes are non-destructive and are reversible, as long as the amount of current flowing does not reach levels that cause the semiconductor material to overheat and cause thermal damage.

6

Forward and reverse biased characteristics of a Silicon diode

In forward biasing, the positive terminal of battery is connected to the P side and the negative terminal of battery is connected to the N side of the diode. Diode will conduct in forward biasing because the forward biasing will decrease the depletion region width and overcome the barrier potential. In order to conduct, the forward biasing voltage should be greater than the barrier potential. During forward biasing the diode acts like a closed switch with a potential drop of nearly 0.6 V across it for a silicon diode. The forward and reverse bias characteristics of a silicon diode. From the graph, you may notice that the diode starts conducting when the forward bias voltage exceeds around 0.6 volts (for Si diode). This voltage is called cut-in voltage.

In reverse biasing, the positive terminal of battery is connected to the N side and the negative terminal of battery is connected to the P side of a diode. In reverse biasing, the diode does not conduct electricity, since reverse biasing leads to an increase in the depletion region width; hence current carrier charges find it more difficult to overcome the barrier potential. The diode will act like an open switch and there is no current flow.

Diode Equation

In the forward-biased and reversed-biased regions, the current I_f, and the voltage V_f, of a semiconductor diode is related by the diode equation:

$$I_f = I_s\left(exp^{\frac{V_f}{nV_T}} - 1\right)$$

where,

I_s is reverse saturation current or leakage current,

I_f is current through the diode(forward current),

V_f is potential difference across the diode terminals(forward voltage)

V_T is thermal voltage, given by

$$V_T = \frac{kT}{q}$$

and k is Boltzmann's constant = 1.38×10^{-23} J /°Kelvin, q is the electronic charge = 1.6×10^{-19} joules/volt(Coulombs), T is the absolute temperature in °Kelvin(°K = 273 + temperature in °C), At room temperature (25 °C), the thermal voltage is about 25.7 mV, n is an empirical constant between 0.5 and 2

The empirical constant, n, is a number that can vary according to the voltage and current levels. It depends on electron drift, diffusion, and carrier recombination in the depletion region. Among the quantities affecting the value of n are the diode manufacture, levels of doping and purity of materials.

Note

1. Ideal Diode Model: Diode is a simple switch that is either closed (conducting) or open (non conducting). Specifically, the diode is a short circuit, like a closed switch, when voltage is applied in the forward direction, and an open circuit, like an open switch, when the voltage is applied in the reverse direction.

2. Offset Voltage Model: The offset voltage model adds the barrier potential to the ideal switch model. When the diode is forward biased it is equivalent to a closed switch in series with a small equivalent voltage source equal to the barrier potential (0.6 V for Silicon, 0.2 for germanium) with the positive side towards the anode. When the diode is reverse biased, it is equivalent to an open switch just as in the ideal model.

3. Complete diode Model: It is the most accurate of the diode models. The Complete diode model of a diode consists of the barrier potential, the small forward dynamic resistance and the ideal diode. The resistor approximates the semiconductor resistance under forward bias. This diode model most accurately represents the true operating characteristics of the real diode.

4. When a diode is reverse biased a leakage current flows through the device. This current can be effectively ignored as long as the reverse breakdown voltage of the diode is not exceeded. At potentials greater than the reverse breakdown voltage, charge is pulled through the p-n junction by the strong electric fields in the device and large reverse current flows. This usually destroys the device. There are special diodes that are designed to operate in breakdown. Such diodes are called zener diodes and used as voltage regulators.

When is each Model used ?

Ideal Diode Model: This is primarily used in troubleshooting. Is the diode working or not. The greatest utility of the ideal diode model is in determining which diodes are on and which are off in a multi-diode circuit.

Offset Voltage Model: This is used when a more accurate determination of load current or voltage is required.

Complete Diode Model: This is used during the actual design of circuits using diodes.

Procedure

Forward Bias-Si Diode

1. Set DC voltage to 0.2 V .
2. Select the diode.
3. Set the resistor.
4. Voltmeter is placed parallel to Silicon diode and ammeter series with resistor.
5. The positive side of battery to the P side(anode) and the negative of battery to the N side(cathode) of the diode.
6. Now vary the voltage upto 5V and note the Voltmeter and Ammeter reading for particular DC voltage .
7. Take the readings and note Voltmeter reading across Silicon diode and Ammeter reading.
8. Plot the V-I graph and observe the change.
9. Calculate the dynamic resistance of the diode. $r_d=\Delta V/\Delta I$
10. Therefore from the graph we see that the diode starts conducting when the forward bias voltage exceeds around 0.6 volts (for Si diode). This voltage is called cut-in voltage.

Reverse Bias-Si Diode

1. Set DC voltage to 0.2 V .
2. Select the diode.
3. Set the resistor.
4. Voltmeter is placed parallel to Silicon diode and ammeter series with resistor.
5. The positive terminal of battery is connected to the N side(cathode) and the negative terminal of battery is connected to the P side(anode) of a diode.
6. Now vary the voltage upto 30V and note the Voltmeter and Ammeter reading for DC voltage .
7. Take the readings and note Voltmeter reading across Silicon diode and Ammeter reading.
8. **Plot the V-I graph and observe the change.**

EXPERIMENT-2

Objective: To verify the V-I characteristics of the Zener diode.

Apparatus required

Power supply

Lab trainer kit

Jumper wires

Multimeter

Theory

Zener Diode

A Zener Diode is a special kind of diode which permits current to flow in the forward direction as normal, but will also allow it to flow in the reverse direction when the voltage is above the breakdown voltage or 'zener' voltage. Zener diodes are designed so that their breakdown voltage is much lower - for example just 2.4 Volts.
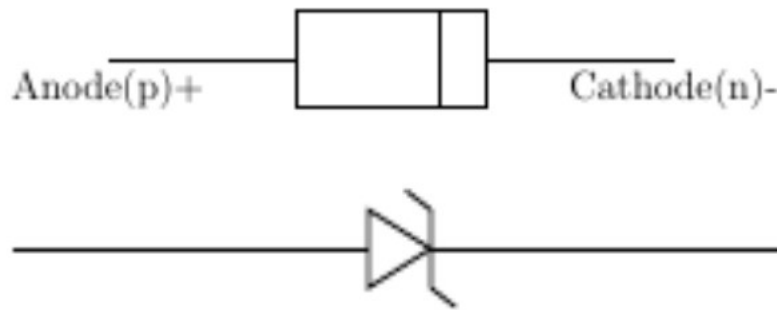

Function of Zener Diode

1. Zener diodes are a special kind of diode which permits current to flow in the forward direction.
2. Zener diodes will also allow current to flow in the reverse direction when the voltage is above a certain value. This breakdown voltage is known as the Zener voltage. In a standard diode, the Zener voltage is high, and the diode is permanently damaged if a reverse current above that value is allowed to pass through it.
3. In the reverse bias direction, there is practically no reverse current flow until the breakdown voltage is reached. When this occurs there is a sharp increase in reverse current. Varying amount of reverse current can pass through the diode without damaging it. The breakdown voltage or zener voltage (VZ) across the diode remains relatively constant.

Zener Diode As A Voltage Regulator

A voltage regulator is an electronic circuit that provides a stable DC voltage independent of the load current, temperature and AC line voltage variations. A Zener diode of break down voltage VZ is reverse connected to an input voltage source V_I across a load resistance R_L and a series resistor R_S. The voltage across the zener will remain steady at its break down voltage V_Z for all the values of zener current I_Z as long as the current remains in the break down region. Hence a regulated DC output voltage $V_0 = V_Z$ is obtained across R_L, whenever the input voltage remains within a minimum and maximum voltage. Basically there are two type of regulations such as: Line Regulation: In this type of regulation, series resistance and load resistance are fixed, only input voltage is changing. Output voltage remains the same as long as the input voltage is maintained above a minimum value. Load Regulation: In this type of regulation, input voltage is fixed and the load resistance is varying. Output volt remains same, as long as the load resistance is maintained above a minimum value.

Line Regulation
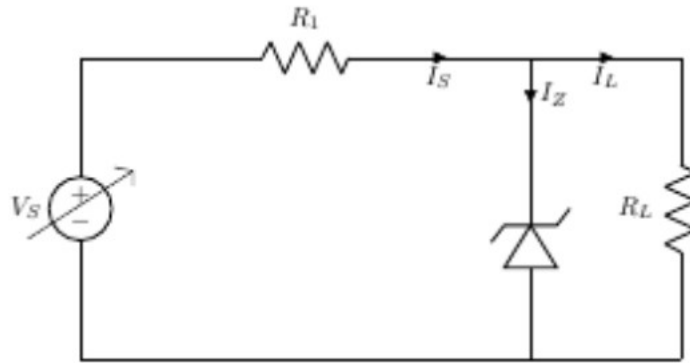
In Line Regulation, Load resistance is constant and input voltage varies. V_I must be sufficiently large to turn the Zener Diode ON.

$$V_L = V_Z = \frac{V_{Imin} \times R_L}{(R_S + R_L)}$$

So, the minimum turn-on voltage V_{Imin} is :

$$V_{Imin} = \frac{V_Z \times (R_S + R_L)}{R_L}$$

The maximum value of V_I is limited by the maximum zener current I_{Zmax}

$$I_{Rmax} = I_{Zmax} + I_L$$

I_L is fixed at :

$$\frac{V_Z}{R_L}$$

Since, $V_L = V_Z$, So maximum V_I is

$$V_{Imax} = V_{Rmax} + V_Z$$

$$V_{Imax} = I_{Rmax} \times R + V_Z$$

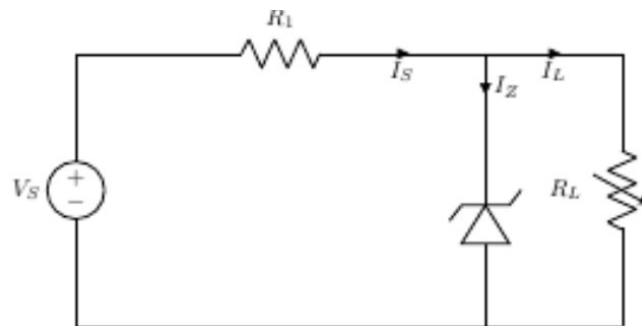For $V_I < V_Z$

$$V_O = V_I$$

For $V_I > V_Z$

$$V_O = V_I - I_S \times R_S$$

Load Regulation

In Load Regulation , input voltage is constant and Load resistance varies. Too small a Load Resistance R_L, will result in $V_{Th} < V_Z$ and Zener Diode will be OFF.

$$V_L = V_Z = \frac{V_{Imin} \times R_L}{(R_S + R_L)}$$

So the minimum load resistance R_L

$$R_{Lmin} = \frac{V_Z \times R_S}{V_I - V_Z}$$

Any load resistance greater than R_{Lmin} will make Zener Diode ON

$$I_S = I_L + I_Z$$

R_{Lmin} will establish maximum I_L as

12

$$I_{Lmax} = \frac{V_L}{R_{Lmin}} = \frac{V_Z}{R_{Lmin}} \qquad Since, V_L = V_Z$$

V_S is the voltage drop across R_S

$$V_S = V_{Imin} - V_Z$$

$$I_S = \frac{V_{Imin} - V_Z}{R_S}$$

For $R_L < R_{Lmin}$

$$V_O = V_I$$

For $R_L > R_{Lmin}$

$$V_O = V_I - I_S \times R_S$$

Procedure

Zener Diode - Line Regulation

1. Set the Zener Voltage(V_Z)
2. Set the Series Resistance (R_S) value.
3. Set the Load Resistance (R_L) value.
4. Vary DC voltage.
5. Voltmeter is placed parallel to load resistor and ammeter series with the series resistor.
6. Choose appropriate DC voltage such that zener diode is 'on'.
7. Now note the Voltmeter and Ammeter reading for various DC voltage.
8. Note the Load current(I_L), zener current(I_Z), Output voltage(V_O)
9. Calculate the voltage regulation.

Zener Diode - Load Regulation

1. Set DC voltage.
2. Set the Series Resistance (R_S) value.
3. 1W D0-41 Glass Zener Diode 1N4740A, Zener voltage is 10 V.
4. Vary the Load Resistance (R_L).
5. Voltmeter is placed parallel to load resistor and ammeter series with the series resistor.
6. Choose Load Resistance in such a manner, such that the Zener diode is 'on'.
7. Now note the Voltmeter and Ammeter reading for various Load Resistance.
8. Increase the load resistance (R_L).
9. Note the Load current (I_L), zener current (I_Z), Output voltage(V_O)
10. Calculate the voltage regulation.

13

EXPERIMENT-3

Objective: To verify the V-I characteristics of the LED.

Apparatus required

Power supply

Lab trainer kit

Jumper wires

Oscilloscope

Waveform generator

Multimeter

Theory

Light Emitting Diode (LED)

A Light Emitting Diode (LED) is a semiconductor diode that emits light when an electric current is applied in forward direction of the device as in simple LED circuit. The effect is a form of electroluminescence where incoherent and narrow-spectrum light is emitted from the p-n junction.

For optical communication systems requiring bit rates less than approximately 100-200 Mb/s together with multimode fiber-coupled optical power in tens of microwatts, semiconductor light-emitting diodes (LEDs) are usually the best light source choice. LEDs require less complex drive circuitry than laser diodes since no thermal or optical stabilization circuits are needed and they can be fabricated less expensively with higher yields.

To be useful in fiber transmission applications and LED must have a high radiance output, a fast emission response time and high quantum efficiency. To achieve a high radiance and a high quantum efficiency, the LED structure must provide a means of confining the charge carriers and the stimulated optical emission to the active region of the pn junction where radiative recombination takes place.

The two basic LED configurations being used for fiber optics are surface emitters and edge emitters.

Internal Quantum Efficiency

 The internal quantum efficiency η_{int} is an important parameter of an LED. It is defined as the fraction of the electron-hole pairs that recombine radiatively. If the radiative recombination rate is R_r and the non-radiative recombination rate is R_{nr}, then the internal quantum efficiency is the ratio is the ratio of the

radaitiverecombination rate to the total recombination rate. ηint is typically 50% in homojunction LEDs, but ranges from 60 to 80% in double-heterostructure LEDs.

Optical Power

If the current injected into the LED is I, then the total number of recombinations per second is I/q, where q is the electron charge. Total number of radaiativerecombinations is equal to (ηint I/q). Since each photon has an energy hv, the optical power generated internally by the LED is: Pint = (ηint I/q)(hv).

External Quantum Efficiency

The external quantum efficiency (ηext)of a LED is defined as the ratio of the photons emitted from the LED to the number of internally generated photons. Due to reflection effects at the surface of the LED typical values of ηout are < 10%.
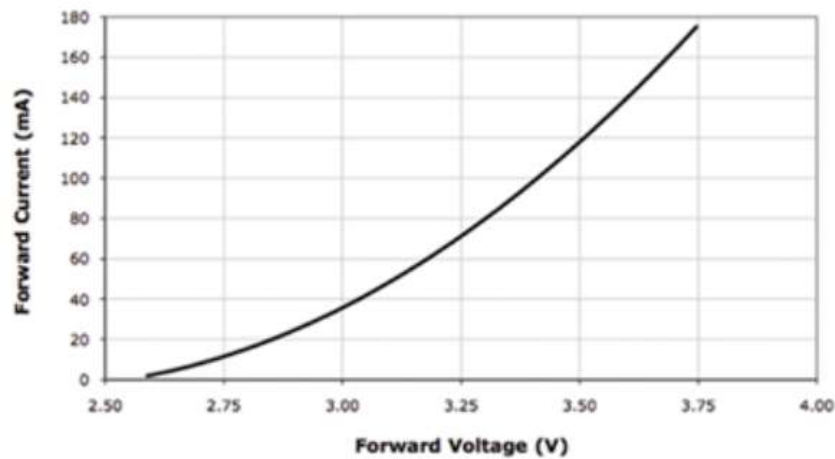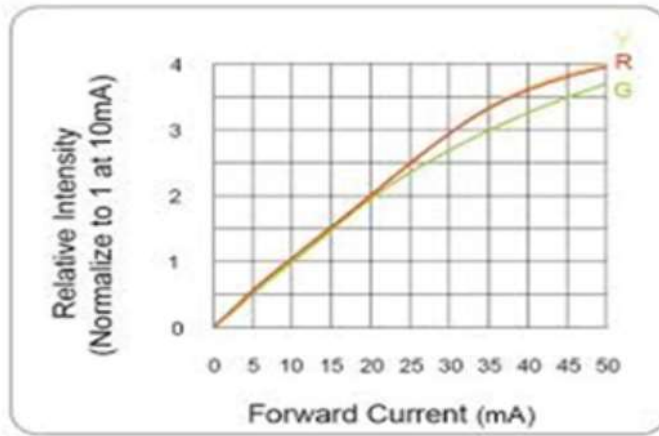
LED Characteristics

Two important characteristics of a LED are its Light intensity vs. Current and Junction Voltage vs. Current characteristics. These are described briefly below.

  i)   Light Intensity (Optical Power) vs. Current

This is a very important characteristic of an LED. It was shown earlier that the optical power generated by an LED is directly proportional to the injected current I (current through the LED). However, in practice the characteristic is generally non-linear, especially at higher currents. The near-linear light output characteristic of an LED is exploited in small length fiber optic analog communication links, such as fiber optic closed-circuit TV.

  ii)   Junction Voltage vs. Current

The junction voltage vs. current characteristic of an LED is similar to the V-I characteristics of diodes. However, there is one major difference. The knee voltage of a diode is related to the barrier potential of the material used in the device. Silicon diodes and bipolar junction transistors are very commonly used whose knee voltage or junction voltage is about 0.7 V. Very often it is wrongly assumed that other diodes also have the same junction voltage. In an LED, depending on the material used its junction voltage can be anywhere between 1.5 to 2.2 Volts.

Relative Intensity (Normalize to 1 at 10mA) vs Forward Current (mA)

Forward Current (mA) vs Forward Voltage (V)

Procedure

Forward Bias-Si Diode

1. Set DC voltage to 0.2 V .
2. Select the diode.
3. Set the resistor.
4. Voltmeter is placed parallel to LED and ammeter series with resistor.
5. The positive side of battery to the P side(anode) and the negative of battery to the N side(cathode) of the diode.
6. Now vary the voltage upto 5V and note the Voltmeter and Ammeter reading for particular DC voltage .
7. Take the readings and note Voltmeter reading across LED and Ammeter reading.
8. Plot the V-I graph and observe the change.

16

EXPERIMENT-4

Objective: To study half-wave, full-wave rectifier and evaluate their efficiency.

Apparatus required

Power supply

Lab trainer kit

Jumper wires

Oscilloscope

Waveform generator

Multimeter

Theory

    A rectifier is a device that converts alternating current (AC) to direct current (DC), a process known as rectification. Rectifiers are essentially of two types – a half wave rectifier and a full wave rectifier.

Half Wave Rectification

    On the positive cycle the diode is forward biased and on the negative cycle the diode is reverse biased. By using a diode we have converted an AC source into a pulsating DC source. In summary we have 'rectified' the AC signal.
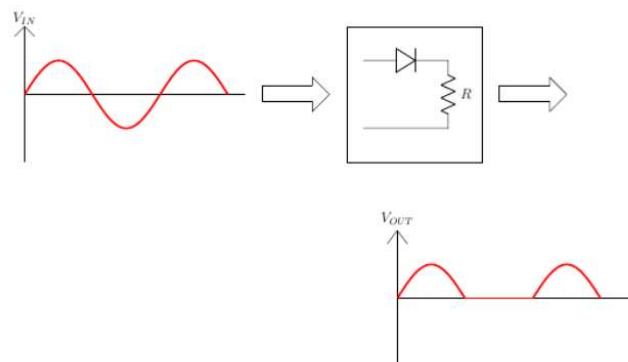
The simplest kind of rectifier circuit is the half-wave rectifier.The half-wave rectifier is a circuit that allows only part of an input signal to pass. The circuit is simply the combination of a single diode in series with a resistor, where the resistor is acting as a load. The output DC voltage of a half wave rectifier can be calculated with the following two ideal equations.

17

$$V_{peak} = V_{rms} \times \sqrt{2}$$

$$V_{dc} = \frac{V_{peak}}{\Pi}$$

<u>Average output voltage</u>

$$V_O = V_m \times \sin wt \quad for \quad 0 \le wt \le \pi$$

$$V_O = 0 \quad for \quad \pi \le wt \le 2\pi$$

$$V_{av} = \frac{V_m}{\pi} = 0.318 V_m$$

RMS load voltage

$$V_{rms} = I_{rms} \times R = \frac{V_m}{2}$$

Average load current

$$I_{av} = \frac{V_{av}}{R} = \frac{\frac{V_m}{\pi}}{R}$$

$$I_{av} = \frac{V_m}{\pi \times R} = \frac{I_m}{\pi}$$

RMS load current

$$I_{rms} = \frac{I_m}{2}$$

Form factor: It is defined as the ratio of rms load voltage and average load voltage.

$$F.F = \frac{V_{rms}}{V_{av}}$$

$$F.F = \frac{\frac{V_m}{2}}{\frac{V_{av}}{2}} = \frac{\pi}{2} = 1.57$$

$$F.F \ge 1$$

$$rms \ge av$$

<u>Ripple Factor</u>

18

$$\gamma = \sqrt{(F.F^2 - 1)} \times 100\%$$

$$\gamma = \sqrt{(1.57^2 - 1)} \times 100\% = 1.21\%$$

<u>Efficiency</u>: It is defined as ratio of dc power available at the load to the input ac power.

$$n\% = \frac{P_{load}}{P_{in}} \times 100\%$$

$$n\% = \frac{I_{dc}^2 \times R}{I_{rms}^2 \times R} \times 100\%$$

$$n\% = \frac{\frac{I_m^2}{\pi^2}}{\frac{I_m^2}{4}} \times 100\% = \frac{4}{\pi^2} \times 100\% = 40.56\%$$

<u>Peak Inverse Volatge</u>

For rectifier applications, peak inverse voltage (PIV) or peak reverse voltage (PRV) is the maximum value of reverse voltage which occurs at the peak of the input cycle when the diode is reverse-biased. The portion of the sinusoidal waveform which repeats or duplicates itself is known as the cycle. The part of the cycle above the horizontal axis is called the positive half-cycle, the part of the cycle below the horizontal axis is called the negative half cycle. With reference to the amplitude of the cycle, the peak inverse voltage is specified as the maximum negative value of the sine-wave within a cycle's negative half cycle.

$$PIV = V$$
$$-V_m + V = 0 \Rightarrow V = V_m$$
$$PIV \geq V_m$$

<u>Procedure</u>
1. Set the resistor RL.
2. Click on 'ON' button to start the experiment.
3. Click on 'Sine Wave' button to generate input waveform
4. Click on 'Oscilloscope' button to get the rectified output.
5. Vary the Amplitude, Frequency, volt/div using the controllers.
6. Click on "Dual" button to observe both the waveform.
7. Channel 1 shows the input sine waveform, Channel 2 shows the output rectified waveform.
8. Calculate the Ripple Factor. Theoretical Ripple Factor= 1.21.

Full Wave Rectifier

A full-wave rectifier is exactly the same as the half-wave, but allows unidirectional current through the load during the entire sinusoidal cycle (as opposed to only half the cycle in the half-wave). A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output. Let us see our half wave rectifier example and deduce the circuit.
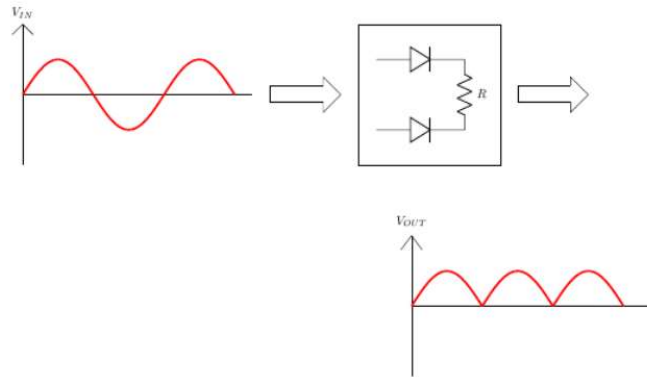

Full Wave Rectifier - Circuit

So, we have seen that this rectifier circuit consists of two sources which have a phase difference along with two diodes. When V_1 is positive, V_2 is negative. Hence the top diode(D_1) will be a short and the bottom diode(D_2) will be an open. On the other hand, when V_1 is negative, V_2 is positive. Hence the bottom diode(D_2) will be on and the top diode(D_1) will be an open circuit. This configuration is rarely used because sometimes it may be impractical to obtain two voltage sources and it is difficult to SYNC the sources. Let us see how a single source can be used.
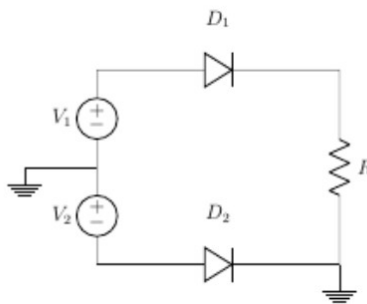
Full Wave Rectifier – Center Tapped Transformer

A Full-Wave Rectifier can be constructed using Center-Tapped transformer – which give us two shifted sinusoids so that exactly one of the waveforms is positive at one time and two diodes. As compared to the half wave rectifier we use two diodes instead of one, one of the two diodes remains in conduction in both of the

halfcycles. At any point in time, only one of the diodes is forward biased. This allows for continuous conduction through load.
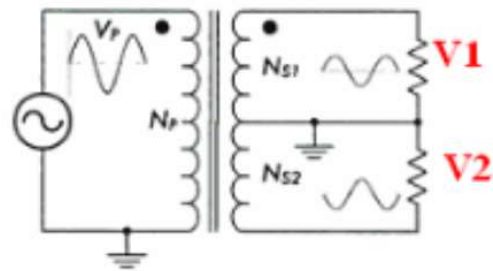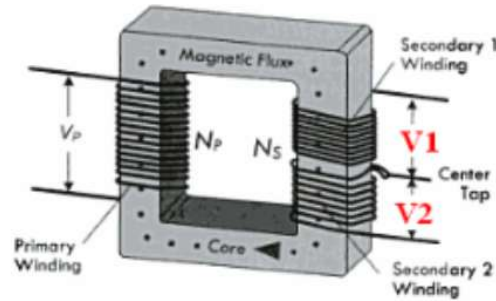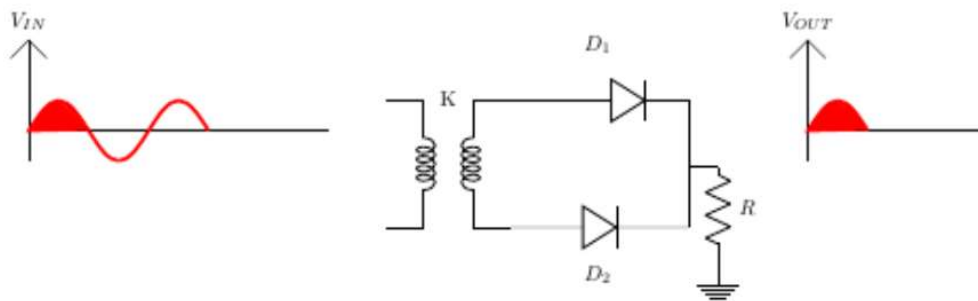

Secondary voltages are 180° out of phase with each other.

$$\frac{N_p}{N_s} = \frac{V_p}{V_s} = \frac{1}{2}$$

$$V_S = 2V_I$$

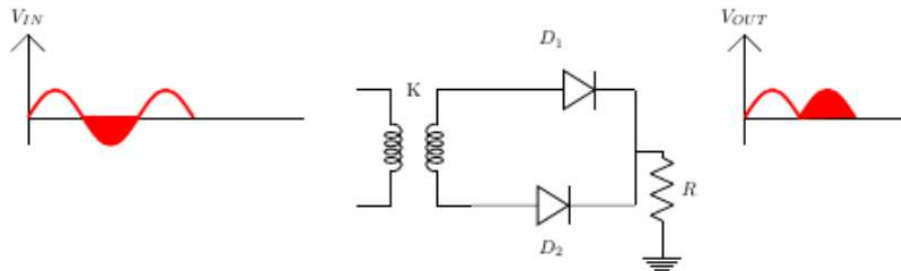Center Tapped Transformer – Positive cycle

For Positive Cycle D_1 is Forward Biased and D_2 is Reverse Biased

21

$$V_I - V_O = 0$$
$$\Rightarrow V_O = V_I$$

Center Tapped Transformer– Negative cycle

For Negative Cycle D1 is Reversed Biased and D2 is Forward Biased

$$V_I - V_O = 0$$
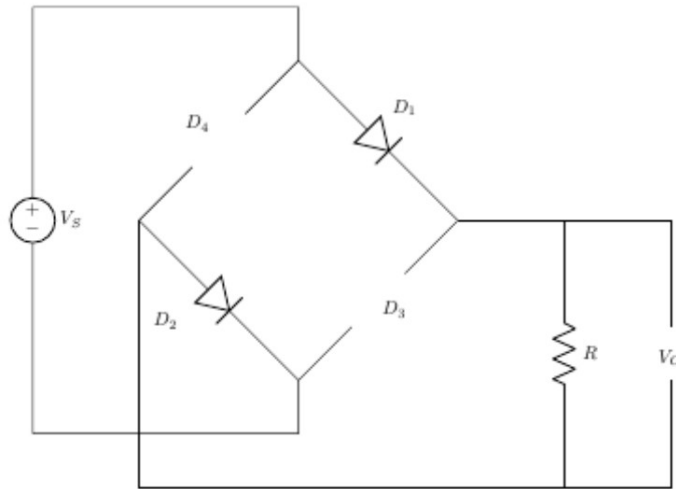$$\Rightarrow V_O = V_I$$

Bridge Rectifier

Bridge rectifier uses 4 rectifying diodes connected in a "bridged" configuration to produce the desired output but does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown below.
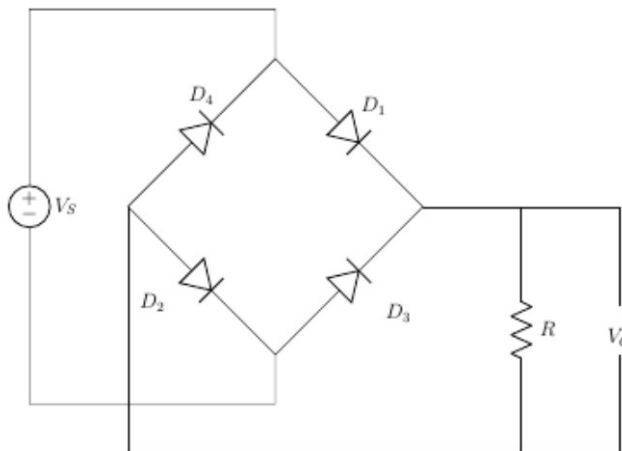
Bridge Rectifier – Positive Half Cycle

During the positive half cycle of the supply diodes D1 and D2 conduct in series while diodes D3 and D4 are reverse biased (ideally they can be replaced with open circuits) and the current flows through the load as shown below.

For Positive Half Cycle D1 and D2 is Forward Biased and D3 and D4 is Reverse Biased.
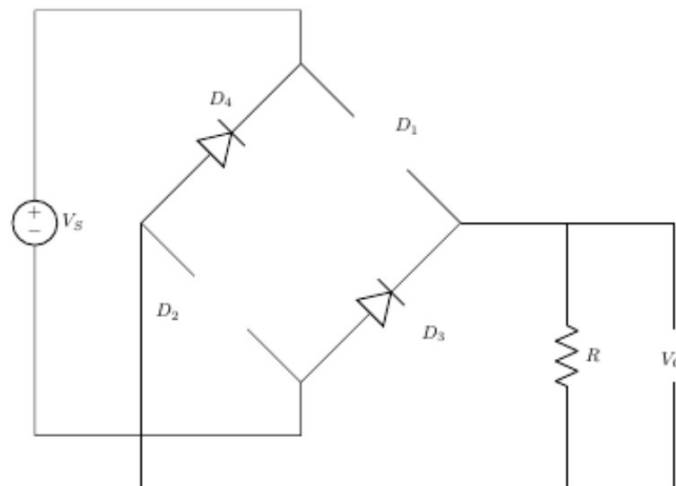
$$V_I - V_O = 0$$
$$\Rightarrow V_O = V_I$$
$$V_O = V_I - 2 \times V_b$$
$$V_O = V_I - 2 \times V_b - 2 \times I_{rd}$$

where, V_I is the input voltage, V_b is barrier potential, r_d is diode resistance.

Bridge Rectifier – Negative Half Cycle

During the negative half cycle of the supply, diodes D3 and D4 conduct in series, but diodes D1 and D2 switch of as they are now reverse biased. The current flowing through the load is the same direction as before.

For Negative Half Cycle D1 and D2 is Reverse Biased and D3 and D4 is Forward Biased.

$$V_I - V_O = 0$$

$$\Rightarrow V_O = V_I$$

Average DC Load Voltage

$$V_O = V_m \times sinwt$$

$$0 \leq wt \leq \pi$$

$$V_{av} = V_{dc} = \frac{2V_m}{\pi}$$

Average Load Current

$$I_{av} = \frac{V_{av}}{R} = \frac{2 \times V_m}{\pi \times R}$$

$$I_{av} = \frac{2 \times I_m}{R}$$

RMS Load Current

$$I = I_m \times sinwt$$

$$0 \leq wt \leq \pi$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

RMS Load Voltage

$$V_{rms} = I_{rms} \times R = \frac{I_m}{\sqrt{2}} \times R$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

Form factor: It is defined as the ratio of rms load voltage and average load voltage.

24

$$F.F = \frac{V_{rms}}{V_{av}}$$

$$F.F = \frac{\frac{V_m}{\sqrt{2}}}{\frac{(2 \times V_m)}{\pi}} = \frac{\pi}{2\sqrt{2}} = 1.11$$

$$F.F \geq 1$$

Ripple Factor

$$\gamma = \sqrt{(F.F^2 - 1)} \times 100\%$$

$$\gamma = \sqrt{(1.11^2 - 1)} \times 100\% = 48.1\%$$

Efficiency: It is defined as ratio of dc power available at the load to the input ac power.

$$n\% = \frac{(I_{dc}^2 \times R)}{(I_{rms}^2 \times R)} \times 100\%$$

$$n\% = \frac{\frac{4 \times I_m^2}{\pi^2}}{\frac{I_m^2}{2}} \times 100\% = \frac{8}{\pi^2} \times 100\% = 81.13$$

Peak Inverse Volatge

For rectifier applications, peak inverse voltage (PIV) or peak reverse voltage (PRV) is the maximum value of reverse voltage which occurs at the peak of the input cycle when the diode is reverse-biased. The portion of the sinusoidal waveform which repeats or duplicates itself is known as the cycle. The part of the cycle above the horizontal axis is called the positive half-cycle, the part of the cycle below the horizontal axis is called the negative half cycle. With reference to the amplitude of the cycle, the peak inverse voltage is specified as the maximum negative value of the sine-wave within a cycle's negative half cycle.

For Bridge Rectifier, D1 and D2 is Forward Biased D3 and D4 is Reverse Biased

$$V_m - V_O = 0$$
$$\Rightarrow V_O = V_m$$
$$V_O + PIV = 0$$
$$PIV = V_m$$
$$PIV \geq V_m$$

For Center Tapped Rectifier, D2 is Forward Biased, PIV at D1,

$$V_m - V_O = 0$$

$$\Rightarrow V_O = V_m$$

$$V_O - PIV + V_m$$

$$\Rightarrow PIV = 2V_m$$

$$PIV \geq 2Vm$$

Procedure

1. Set the resistor RL.
2. Click on 'ON' button to start the experiment.
3. Click on 'Sine Wave' button to generate input waveform
4. Click on 'Oscilloscope' button to get the rectified output.
5. Vary the Amplitude, Frequency, volt/div using the controllers.
6. Click on "Dual" button to observe both the waveform.
7. Channel 1 shows the input sine waveform, Channel 2 shows the output rectified waveform.
8. Calculate the Ripple Factor.Theoretical Ripple Factor= 0.483.

<h1 style="text-align:center">EXPERIMENT-5</h1>

Objective: To study the filter and evaluate the efficiency.

Apparatus required

Power supply

Lab trainer kit

Jumper wires

Oscilloscope

Waveform generator

Multimeter

Theory

Rectifier

In our earlier experiment we have seen that a full-wave rectifier is exactly the same as the half-wave, but allows unidirectional current through the load during the entire sinusoidal cycle (as opposed to only half the cycle in the half-wave). A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output.

Filter

What is really desired is to convert the pulsating output of the rectifier to a constant DC supply. Thus we would like to 'filter' the pulsating input signal.
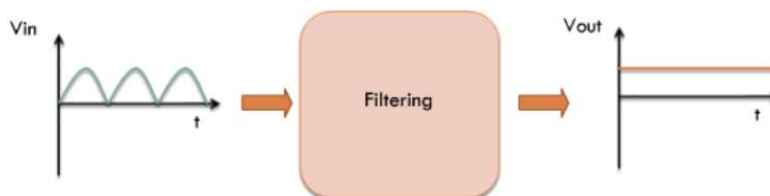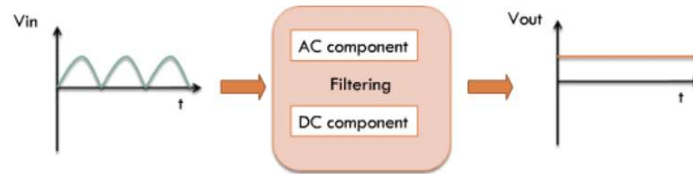
We can do this by splitting the input waveform into AC (high frequency) and the DC components (very low frequency) and by then 'rejecting' the high frequency components.

Filtering

From our filtering experiments we have seen that the simplest kind of filter that can perform the filtering task just described is a capacitor. Thus, if we connect a capacitor directly across the output of a rectifier, the AC components will 'see' a low impedance path to ground and will not, therefore appear in the output.


Full Wave Rectification + Filtering

The smoothing capacitor converts the full-wave rippled output of the rectifier into a smooth DC output voltage. The smoothing capacitor acts as a tank.
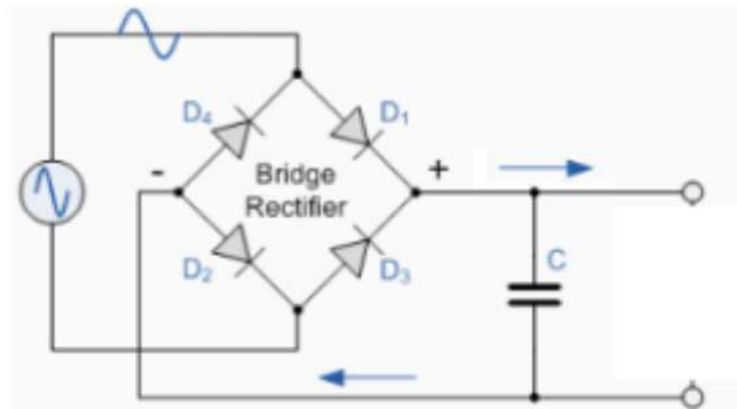
Ripple Voltage and Ripple Factor

Assuming a finite capacitor is connected, since a new charging pulse occurs every half cycle the capacitor charges and discharges very frequently. We can observe that smaller the Vpp, the more the waveform will resemble a pure DC voltage. The variable portion is known as 'ripple' and the value Vpp is known as the ripple voltage. Further the ratio of the ripple voltage to the DC or average voltage is known as the ripple factor.

Rectifier output without smoothing capacitor
Rectifier output with smoothing capacitor
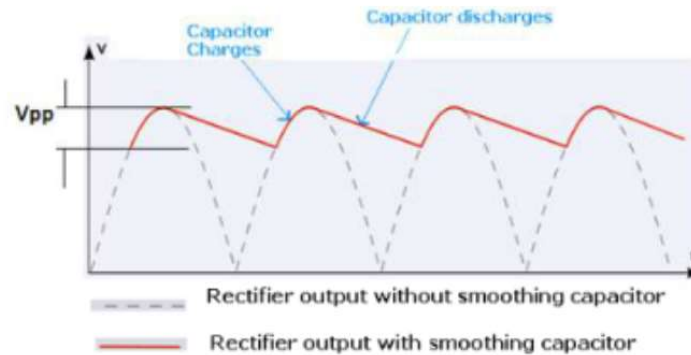
Procedure

Capacitative Rectification for Half Wave Rectifier

1. Take a diode, and Load resistor of 1KOhms and capacitor of 102μF.
2. Connect to AC Voltage Source of 50 Hz, 2 V
3. Click on 'ON' button to make the circuit on.
4. Click on 'Sine Wave' button to observe the input waveform.
5. Click on 'Run Simulation' button to observe the filtered waveform.
6. Observe the corresponding waveform.
7. Channel 1 shows the input wave, Channel 2 shows the output wave and Dual shows both the input and output wave.

Capacitative Rectification for Full Wave Rectifier

1. Take 4 diodes, Load resistor of 1KOhms and capacitor of 102μF.
2. Connect to AC Voltage Source of 50 Hz, 12 V.
3. Click on 'ON' button to make the circuit on.
4. Click on 'Sine Wave' button to observe the input waveform.
5. Click on 'Run Simulation' button to observe the filtered waveform.
6. Vary the amplitude using the controllers.
7. Observe the corresponding waveform.
8. Channel 1 shows the input wave, Channel 2 shows the output wave and Dual shows both the input and output wave.

<h1 style="text-align:center">EXPERIMENT-6</h1>

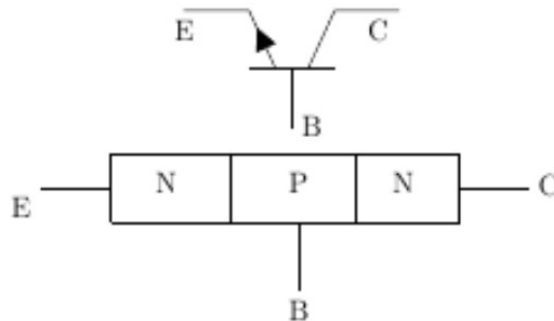**Objective:** **To verify V-I characteristics of BJT in CE–mode.**

Apparatus required

Power supply

Lab trainer kit

Jumper wires

Oscilloscope

Waveform generator

Multimeter

Theory

Structure of Bipolar Junction Transistor

A bipolar junction transistor, BJT, is a single piece of silicon with two back-to-back P-N junctions.BJTs can be made either as PNP or as NPN. They have three regions and three terminals, emitter, base, and collector represented by E, B, and C respectively. The direction of the arrow indicates the direction of the current in the emitter when the transistor is conducting normally. An easy way to remember this is NPN stands for "Not Pointing iN".

Emitter (E): It is the region to the left end which supply free charge carriers i.e., electrons in n-p-n or holes in p-n-p transistors. These majority carriers are injected to the middle region i.e. electrons in the p region of n-p-n or holes in the n region of p-n-p transistor. Emitter is a heavily doped region to supply a large number of majority carriers into the base. **Base (B):** It is the middle region where either two p-type layers or two n-type layers are sandwiched. The majority carriers from the emitter region are injected into this region. This region is thin and very lightly doped. **Collector (C):** It is the region to right end where charge carriers are collected. The area of this region is largest compared to emitter and base region. The doping level of this region is intermediate between heavily doped emitter region and lightly doped base region.

Note

1. In digital electronics applications,the transistors are used as a switch.
2. Most bipolar switching circuits use NPN transistors.

Operation of Bipolar Junction Transistor

Cutoff Region: Base-emitter junction is reverse biased. No current flow. **Saturation Region:** Base-emitter junction is forward biased and Collector-base junction is forward biased. **Active Region:** Base-emitter is junction forward biased and Collector-base junction is reverse biased. **Breakdown Region:** IC and VCE exceed specifications and can cause damage to the transistor.

Cut-Off Region

In Cut-Off region both junctions are reverse biased, Base-emitter junction is reverse biased (VBE<0)and also Collector-Base junction is reverse biased(VCB>0).With reverse biasing, all currents are zero.There are some leakage currents associated with reverse biased junctions,but these currents are small and therefore can be neglected. Application: Open switch

		BE Junction	
		Reverse	Forward
BC Junction	Reverse	Cut-Off	Forward Active
	Forward	Reverse Active	Saturation

Forward Active Region

In Forward Active region Base-emitter junction is forward biased (VBE<0) and Collector-Base junction is reverse biased(VCB<0). In this case, the forward bias of the BE junction will cause the injection of both holes and electrons across the junction. The holes are of little consequence because the doping levels are adjusted to minimize the hole current. The electrons are the carriers of interest. The electrons are injected into the base region where they are called the minority carrier even though they greatly outnumber the holes. Application: Amplifier in analog circuits

$$I_C = -\alpha_F \times I_E + I_{CO}$$

where, α_F is the forward current transfer ratio ICO is Collector reverse saturation current

31

Saturation Region

In Saturation region both junctions are Forward biased,Base-emitter junction is forward biased(VBE>0) and also Collector-Base junction is forward biased(VCB<0). Maximum currents flows through the transistor with only a small voltage drop across the collector junction.The transistor also does not respond to any change in emitter current or base-emitter voltage. Application: Closed switch

Reverse Active Region

In Reverse Active region Base-emitter junction is reverse biased(VBE<0) and Collector-Base junction is forward biased(VCB<0).The operation is just the same as the forward active region, except all voltage sources, and hence collector and emitter currents, are the reverse of the forward bias case. The current gain in this mode is smaller than that of forward active mode for which this mode in general unsuitable for amplification. Application: In digital circuits and analog switching circuits.

$$I_E = -\alpha_R * I_C + I_{EO}$$

where, α_R is the reverse current transfer ratio\newline IEO is the Emitter reverse saturation current

This configuration is rarely used because most transistors are doped selectively to give forward current transfer ratios very near unity, which automatically causes the reverse current transfer ratio to be very low.

BJT -Common Emitter Circuit

The DC behavior of the BJT can be described by the Ebers-Moll Model. The equations for the model are:

$$I_F = I_{ES}(exp^{\frac{V_{BE}}{V_T}} - 1)$$

$$I_R = I_{CS}(exp^{\frac{V_{CB}}{V_T}} - 1)$$

where I_{ES} is base-emitter saturation currents, I_{CS} is base-collector saturation currents

$$V_T = \frac{kT}{q}$$

where, k is the Boltzmann's constant (k = 1.381 e-23 V.C/ K), T is the absolute temperature in degrees Kelvin, and q is the charge of an electron (q = 1.602 e-19 C).

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F}$$

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R}$$

where, β_F is large signal forward current gain of common-emitter configuration, β_R is the large signal reverse current gain of the common-emitter configuration

$$\alpha_F = \frac{\beta_F}{1 + \beta_F}$$

$$\alpha_R = \frac{\beta_R}{1 + \beta_R}$$

where, α_R is large signal reverse current gain of a common-base configuration, α_F is large signal forward current gain of the common-base configuration.

$$I_C = \alpha_F \times I_F - I_R$$

$$I_E = -I_F + \alpha_R * I_R$$

$$I_B = (1 - \alpha_F) \times I_F + (1 - \alpha_R) \times I_R$$

The forward and reverse current gains are related by the expression

$$\alpha_R \times I_{CS} = \alpha_F \times I_{ES} = I_S$$

where, I_S is the BJT transport saturation current. The parameters α_R and α_F are influenced by impurity concentrations and junction depths. The saturation current, I_S, can be expressed as
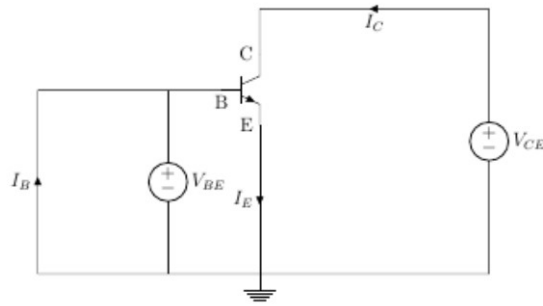
$$I_S = J_S \times A$$

where, A is the area of the emitter and J_S is the transport saturation current density.

Input Characteristics

The most important characteristic of the BJT is the plot of the base current, I_B, versus the base-emitter voltage, V_{BE}, for various values of the collector-emitter voltage, V_{CE}

$$I_B = \phi(V_{BE}, V_{CE})$$
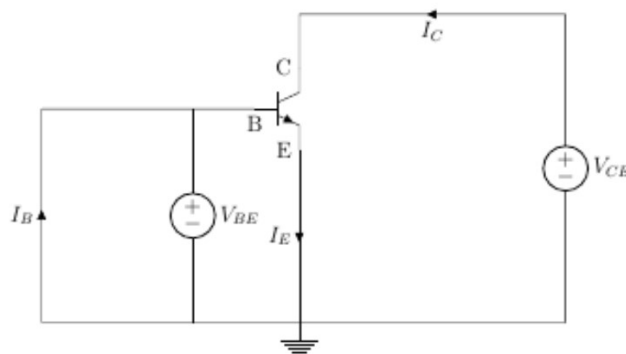
33

for constant V_{CE}

Output Characteristics

The most important characteristic of the BJT is the plot of the collector current, I_C, versus the collector-emitter voltage, V_{CE}, for various values of the base current, I_B as shown on the circuit on the right.

$$I_C = \phi(V_{CE}, I_B)$$

for constant I_B

Procedure

BJT Common Emitter - Input Characteristics

1. Initially set rheostat $R_{h1} = 1\ \Omega$ and rheostat $R_{h2} = 1\ \Omega$
2. Set the Collector-Emitter Voltage(V_{CE}) to 1 V by adjusting the rheostat Rh2
3. Base Emitter Voltage(V_{BE}) is varied by adjusting the rheostat Rh1.
4. Note the reading of Base current(I_B)in micro Ampere.
5. Click on 'Plot' to plot the I-V characteristics of Common-Emitter configuration. A graph is drawn with V_{BE} along X-axis and I_B along Y-axis.
6. Click on 'Clear' button to take another sets of readings
7. Now set the Collector-Emitter Voltage(V_{CE}) to 2 V, 3 V, 4 V

34

BJT Common Emitter - Output Characteristics

1. Initially set rheostat R_{h1} = 1 Ω and rheostat R_{h2} = 1 Ω
2. Set the Base current(I_B)15 uA by adjusting the rheostat R_{h1}
3. Vary the Collector-Emitter Voltage(V_{CE})is varied by adjusting the rheostat R_{h2}.
4. Note the reading of Collector current(I_C).
5. Click on 'Plot' to plot the I-V characteristics of Common-Emitter configuration. A graph is drawn with V_{CE} along X-axis and I_C along Y-axis.
6. Click on 'Clear' button to take another sets of readings
7. Now set the Base Current(I_B) to 20 uA

BJT Common Emitter Amplifier

The common emitter configuration is widely used as a basic amplifier as it has both voltage and current amplification. Resistors R_{B1} and R_{B2} form a voltage divider across the base of the transistor. The function of this network is to provide necessary bias condition and ensure that emitter-base junction is operating in the proper region.

In order to operate transistor as an amplifier, biasing is done in such a way that the operating point is in the active region. For an amplifier the Q-point is placed so that the load line is bisected. Therefore, in practical design V_{CE} is always set to V_{CC}/2. This will confirm that the Q-point always swings within the active region. This limitation can be explained by maximum signal handling capacity. For the maximum input signal, output is produced without any distortion and clipping.

The Bypass Capacitor

The emitter resistor RE is required to obtain the DC quiescent point stability. However the inclusion of RE in the circuit causes a decrease in amplification at higher frequencies. In order to avoid such a condition, it is bypassed by a capacitor so that it acts as a short circuit for AC and contributes stability for DC quiescent condition. Hence capacitor is connected in parallel with emitter resistance.

$$X_{CE} \ll R_E$$

$$\frac{1}{2\pi f C_E} \ll R_E$$

$$C_E \gg \frac{1}{2\pi f R_E}$$

The Input/ Output Coupling (or Blocking) Capacitor

35

An amplifier amplifies the given AC signal. In order to have noiseless transmission of a signal (without DC), it is necessary to block DC i.e. the direct current should not enter the amplifier or load. This is usually accomplished by inserting a coupling capacitor between two stages.

$$X_{CC} \ll R_i h_{ie}$$

$$\frac{1}{2\pi f C_C} \ll R_i h_{ie}$$

$$C_C \gg \frac{1}{2\pi f (R_i h_{ie})}$$

C_C - Output Coupling Capacitor, C_B - Input Coupling Capacitor

## Frequency response of Common Emitter Amplifier

Emitter bypass capacitors are used to short circuit the emitter resistor and thus increases the gain at high frequency. The coupling and bypass capacitors cause the fall of the signal in the low frequency response of the amplifier because their impedance becomes large at low frequencies. The stray capacitances are effectively open circuits. In the mid frequency range large capacitors are effectively short circuits and the stray capacitors are open circuits, so that no capacitance appears in the mid frequency range. Hence the mid band frequency gain is maximum. At the high frequencies, the bypass and coupling capacitors are replaced by short circuits. The stray capacitors and the transistor determine the response.

The input resistance is medium and is essentially independent of the load resistance R_L . The output resistance is relatively high and is essentially independent of the source resistance.

The coupling capacitor, C_{C1} , couples the source voltage V_S to the biasing network. Coupling capacitor C_{C2} connects the collector resistance R_C to the load R_L . The bypass capacitance C_E is used to increase the midband gain, since it effectively short circuits the emitter resistance R_E at midband frequencies. The resistance R_E is needed for bias stability. The external capacitors C_{C1}, C_{C2}, C_E will influence the low frequency response of the common emitter amplifier. The internal capacitances of the transistor will influence the high frequency cut-off.

$$A(s) = \frac{A_m S^2 (S + w_Z)}{(S + w_{L1})(S + w_{L2})(S + w_{L3})(1 + \frac{S}{w_H})}$$

where, A_M is the midband gain, ω_H is the frequency of the dominant high frequency pole,
ω_{L1}, ω_{L2}, ω_{L3} are low frequency poles introduced by the coupling and bypass capacitors,
w_Z is the zero introduced by the bypass capacitor. The midband gain is obtained by short circuiting all the external capacitors and open circuiting the internal capacitors.

36
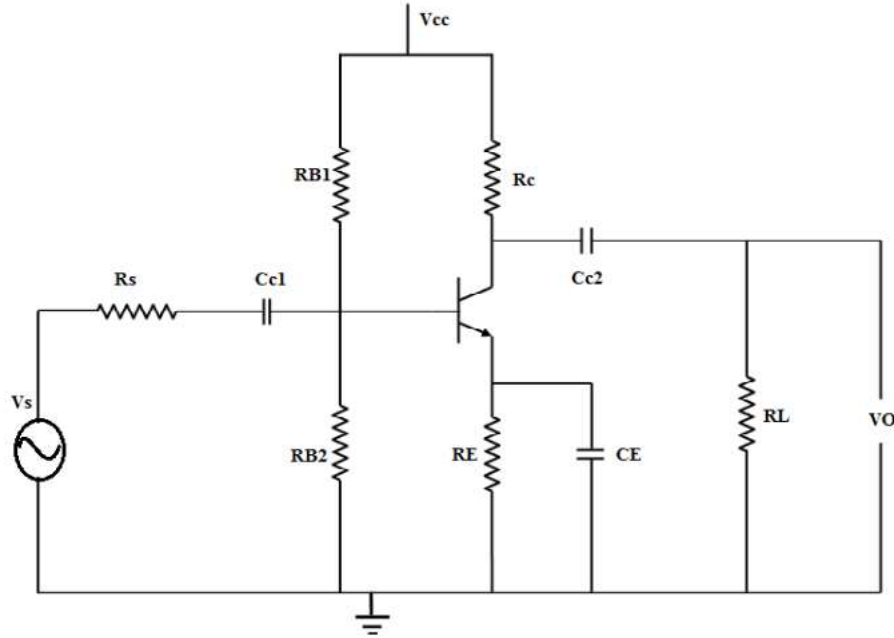
Procedure

1. The source voltage (V_S) is set to 50mV at 1 KHz frequency.
2. Keeping source voltage constant, vary the frequency from 50 Hz in regular steps.
3. Set Source Resistance(R_S)=100Ω.
4. Set Collector Resistance(R_C)=4000Ω, Set Emitter Resistance(R_E)=1000Ω, Set Load Resistance(R_L)=2000Ω.
5. Set Base Resistance1(R_{B1})=47 KΩ, Set Base Resistance2(RB2)=10KΩ.
6. Set Coupling Capacitor1(C_{C1})=10μF, Set Coupling Capacitor2(C_{C2}) =10μF, Set Bypass Capacitance(C_E)=10μF.
7. Vary the Frequency by keeping the resistances constant.
8. Plot the Magnitude graph of the CE Amplifier, Frequency(Hz) along X-axis and Magnitude(dB) along Y-axis.

<center>**EXPERIMENT-7**</center>

Objective: To verify V-I characteristics of BJT in CB–mode.

Apparatus required

Power supply

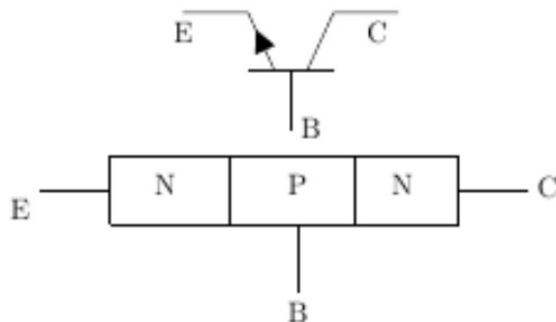Lab trainer kit

Jumper wires

Oscilloscope

Waveform generator

Multimeter

Theory

Structure of Bipolar Junction Transistor

A bipolar junction transistor, BJT, is a single piece of silicon with two back-to-back P-N junctions.BJTs can be made either as PNP or as NPN. They have three regions and three terminals, emitter, base, and collector represented by E, B, and C respectively. The direction of the arrow indicates the direction of the current in the emitter when the transistor is conducting normally. An easy way to remember this is NPN stands for "Not Pointing iN".

Emitter (E): It is the region to the left end which supply free charge carriers i.e., electrons in n-p-n or holes in p-n-p transistors. These majority carriers are injected to the middle region i.e. electrons in the p region of n-p-n or holes in the n region of p-n-p transistor. Emitter is a heavily doped region to supply a large number of majority carriers into the base. **Base (B):** It is the middle region where either two p-type layers or two n-type layers are sandwiched. The majority carriers from the emitter region are injected into this region. This region is thin and very lightly doped. **Collector (C):** It is the region to right end where charge carriers are collected. The area of this region is largest compared to emitter and base region. The doping level of this region is intermediate between heavily doped emitter region and lightly doped base region.

38

Note

1. In digital electronics applications,the transistors are used as a switch.
2. Most bipolar switching circuits use NPN transistors.

Operation of Bipolar Junction Transistor

Cutoff Region: Base-emitter junction is reverse biased. No current flow. **Saturation Region:** Base-emitter junction is forward biased and Collector-base junction is forward biased. **Active Region:** Base-emitter is junction forward biased and Collector-base junction is reverse biased. **Breakdown Region:** IC and VCE exceed specifications and can cause damage to the transistor.

Cut-Off Region

In Cut-Off region both junctions are reverse biased, Base-emitter junction is reverse biased (VBE<0)and also Collector-Base junction is reverse biased(VCB>0).With reverse biasing, all currents are zero.There are some leakage currents associated with reverse biased junctions,but these currents are small and therefore can be neglected. Application: Open switch

	BE Junction	
	Reverse	Forward
BC Junction Reverse	Cut-Off	Forward Active
BC Junction Forward	Reverse Active	Saturation

Forward Active Region

In Forward Active region Base-emitter junction is forward biased (VBE<0) and Collector-Base junction is reverse biased(VCB<0). In this case, the forward bias of the BE junction will cause the injection of both holes and electrons across the junction. The holes are of little consequence because the doping levels are adjusted to minimize the hole current. The electrons are the carriers of interest. The electrons are injected into the base region where they are called the minority carrier even though they greatly outnumber the holes. Application: Amplifier in analog circuits

$$I_C = -\alpha_F \times I_E + I_{CO}$$

where, α_F is the forward current transfer ratio ICO is Collector reverse saturation current

Saturation Region

In Saturation region both junctions are Forward biased,Base-emitter junction is forward biased(VBE>0) and also Collector-Base junction is forward biased(VCB<0). Maximum currents flows through the transistor with only a small voltage drop across the collector junction.The transistor also does not respond to any change in emitter current or base-emitter voltage. Application: Closed switch

Reverse Active Region

In Reverse Active region Base-emitter junction is reverse biased(VBE<0) and Collector-Base junction is forward biased(VCB<0).The operation is just the same as the forward active region, except all voltage sources, and hence collector and emitter currents, are the reverse of the forward bias case. The current gain in this mode is smaller than that of forward active mode for which this mode in general unsuitable for amplification. Application: In digital circuits and analog switching circuits.

$$I_E = -\alpha_R * I_C + I_{EO}$$

where, α_R is the reverse current transfer ratio\newline IEO is the Emitter reverse saturation current

This configuration is rarely used because most transistors are doped selectively to give forward current transfer ratios very near unity, which automatically causes the reverse current transfer ratio to be very low.

BJT -Common Base Circuit

The DC behavior of the BJT can be described by the Ebers-Moll Model. The equations for the model are:

$$I_F = I_{ES}(exp^{\frac{V_{BE}}{V_T}} - 1)$$

$$I_R = I_{CS}(exp^{\frac{V_{CB}}{V_T}} - 1)$$

where I_{ES} is base-emitter saturation currents, I_{CS} is base-collector saturation currents

$$V_T = \frac{kT}{q}$$

where, k is the Boltzmann's constant (k = 1.381 e-23 V.C/ K), T is the absolute temperature in degrees Kelvin, and q is the charge of an electron (q = 1.602 e-19 C).

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F}$$

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R}$$

where, β_F is large signal forward current gain of common-emitter configuration, β_R is the large signal reverse current gain of the common-emitter configuration

$$\alpha_F = \frac{\beta_F}{1 + \beta_F}$$

$$\alpha_R = \frac{\beta_R}{1 + \beta_R}$$

where, α_R is large signal reverse current gain of a common-base configuration, α_F is large signal forward current gain of the common-base configuration.

$$I_C = \alpha_F \times I_F - I_R$$

$$I_E = -I_F + \alpha_R * I_R$$

$$I_B = (1 - \alpha_F) \times I_F + (1 - \alpha_R) \times I_R$$

The forward and reverse current gains are related by the expression

$$\alpha_R \times I_{CS} = \alpha_F \times I_{ES} = I_S$$

where, I_S is the BJT transport saturation current. The parameters α_R and α_F are influenced by impurity concentrations and junction depths. The saturation current, I_S, can be expressed as
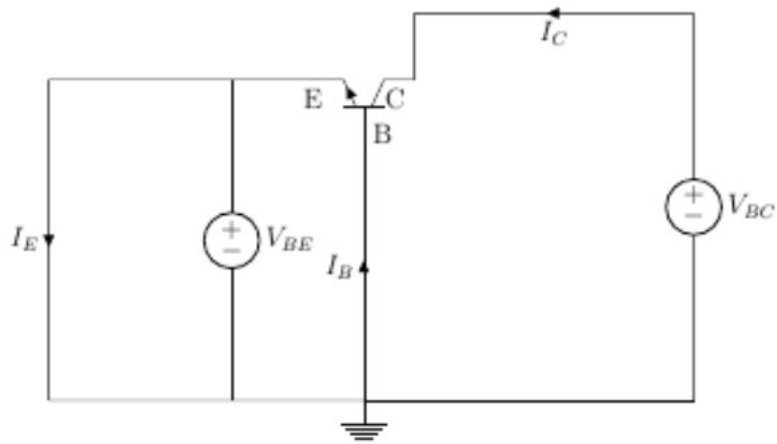
$$I_S = J_S \times A$$

where, A is the area of the emitter and J_S is the transport saturation current density.

Input Characteristics

The most important characteristic of the BJT is the plot of the emitter current, IE, versus the base-emitter voltage,VBE, for various values of the collector-base voltage,VCB

$$I_B = \phi(V_{BE}, V_{CE})$$

for constant V_{CB}

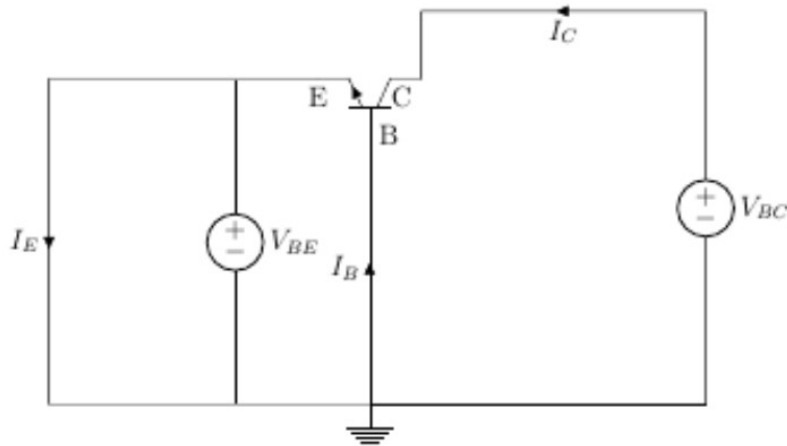## Output Characteristics

The most important characteristic of the BJT is the plot of the collector current, IC, versus the collector-base voltage, VCB, for various values of the emitter current, IE as shown on the circuit on the right.

$$I_C = \phi(V_{CE}, I_E)$$

for constant I_E

<div align="center">

EXPERIMENT-8

</div>

Objective: **To verify V-I characteristics of BJT in CC–mode.**

Apparatus required

Power supply

Lab trainer kit

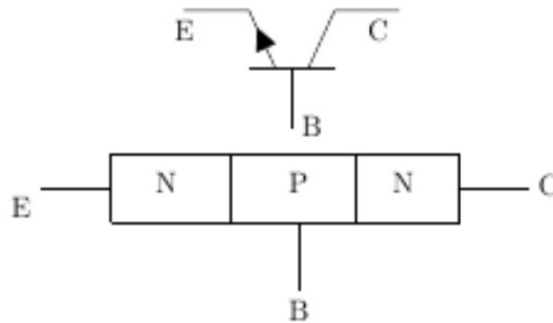Jumper wires

Oscilloscope

Waveform generator

Multimeter

Theory

Structure of Bipolar Junction Transistor

A bipolar junction transistor, BJT, is a single piece of silicon with two back-to-back P-N junctions.BJTs can be made either as PNP or as NPN. They have three regions and three terminals, emitter, base, and collector represented by E, B, and C respectively. The direction of the arrow indicates the direction of the current in the emitter when the transistor is conducting normally. An easy way to remember this is NPN stands for "Not Pointing iN".

Emitter (E): It is the region to the left end which supply free charge carriers i.e., electrons in n-p-n or holes in p-n-p transistors. These majority carriers are injected to the middle region i.e. electrons in the p region of n-p-n or holes in the n region of p-n-p transistor. Emitter is a heavily doped region to supply a large number of majority carriers into the base. **Base (B):** It is the middle region where either two p-type layers or two n-type layers are sandwiched. The majority carriers from the emitter region are injected into this region. This region is thin and very lightly doped. **Collector (C):** It is the region to right end where charge carriers are collected. The area of this region is largest compared to emitter and base region. The doping level of this region is intermediate between heavily doped emitter region and lightly doped base region.

Note
1. In digital electronics applications,the transistors are used as a switch.
2. Most bipolar switching circuits use NPN transistors.

Operation of Bipolar Junction Transistor

Cutoff Region: Base-emitter junction is reverse biased. No current flow. **Saturation Region:** Base-emitter junction is forward biased and Collector-base junction is forward biased. **Active Region:** Base-emitter is junction forward biased and Collector-base junction is reverse biased. **Breakdown Region:** IC and VCE exceed specifications and can cause damage to the transistor.

Cut-Off Region

In Cut-Off region both junctions are reverse biased, Base-emitter junction is reverse biased (VBE<0)and also Collector-Base junction is reverse biased(VCB>0).With reverse biasing, all currents are zero.There are some leakage currents associated with reverse biased junctions,but these currents are small and therefore can be neglected. Application: Open switch

BE Junction

		Reverse	Forward
BC Junction	Reverse	Cut-Off	Forward Active
	Forward	Reverse Active	Saturation

Forward Active Region

In Forward Active region Base-emitter junction is forward biased (VBE<0) and Collector-Base junction is reverse biased(VCB<0). In this case, the forward bias of the BE junction will cause the injection of both holes and electrons across the junction. The holes are of little consequence because the doping levels are adjusted to minimize the hole current. The electrons are the carriers of interest. The electrons are injected into the base region where they are called the minority carrier even though they greatly outnumber the holes. Application: Amplifier in analog circuits

$$I_C = -\alpha_F \times I_E + I_{CO}$$

where, α_F is the forward current transfer ratio ICO is Collector reverse saturation current

Saturation Region

In Saturation region both junctions are Forward biased,Base-emitter junction is forward biased(VBE>0) and also Collector-Base junction is forward biased(VCB<0). Maximum currents flows through the transistor with only a small voltage drop across the collector junction.The transistor also does not respond to any change in emitter current or base-emitter voltage. Application: Closed switch

Reverse Active Region

In Reverse Active region Base-emitter junction is reverse biased(VBE<0) and Collector-Base junction is forward biased(VCB<0).The operation is just the same as the forward active region, except all voltage sources, and hence collector and emitter currents, are the reverse of the forward bias case. The current gain in this mode is smaller than that of forward active mode for which this mode in general unsuitable for amplification. Application: In digital circuits and analog switching circuits.

$$I_E = -\alpha_R * I_C + I_{EO}$$

where, α_R is the reverse current transfer ratio\newline IEO is the Emitter reverse saturation current

This configuration is rarely used because most transistors are doped selectively to give forward current transfer ratios very near unity, which automatically causes the reverse current transfer ratio to be very low.

BJT -Common Base Circuit

The DC behavior of the BJT can be described by the Ebers-Moll Model. The equations for the model are:

$$I_F = I_{ES}(exp^{\frac{V_{BE}}{V_T}} - 1)$$

$$I_R = I_{CS}(exp^{\frac{V_{CB}}{V_T}} - 1)$$

where I_{ES} is base-emitter saturation currents, I_{CS} is base-collector saturation currents

$$V_T = \frac{kT}{q}$$

where, k is the Boltzmann's constant (k = 1.381 e-23 V.C/ K), T is the absolute temperature in degrees Kelvin, and q is the charge of an electron (q = 1.602 e-19 C).

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F}$$

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R}$$

where, β_F is large signal forward current gain of common-emitter configuration, β_R is the large signal reverse current gain of the common-emitter configuration

$$\alpha_F = \frac{\beta_F}{1 + \beta_F}$$

$$\alpha_R = \frac{\beta_R}{1 + \beta_R}$$

where, α_R is large signal reverse current gain of a common-base configuration, α_F is large signal forward current gain of the common-base configuration.

$$I_C = \alpha_F \times I_F - I_R$$

$$I_E = -I_F + \alpha_R * I_R$$

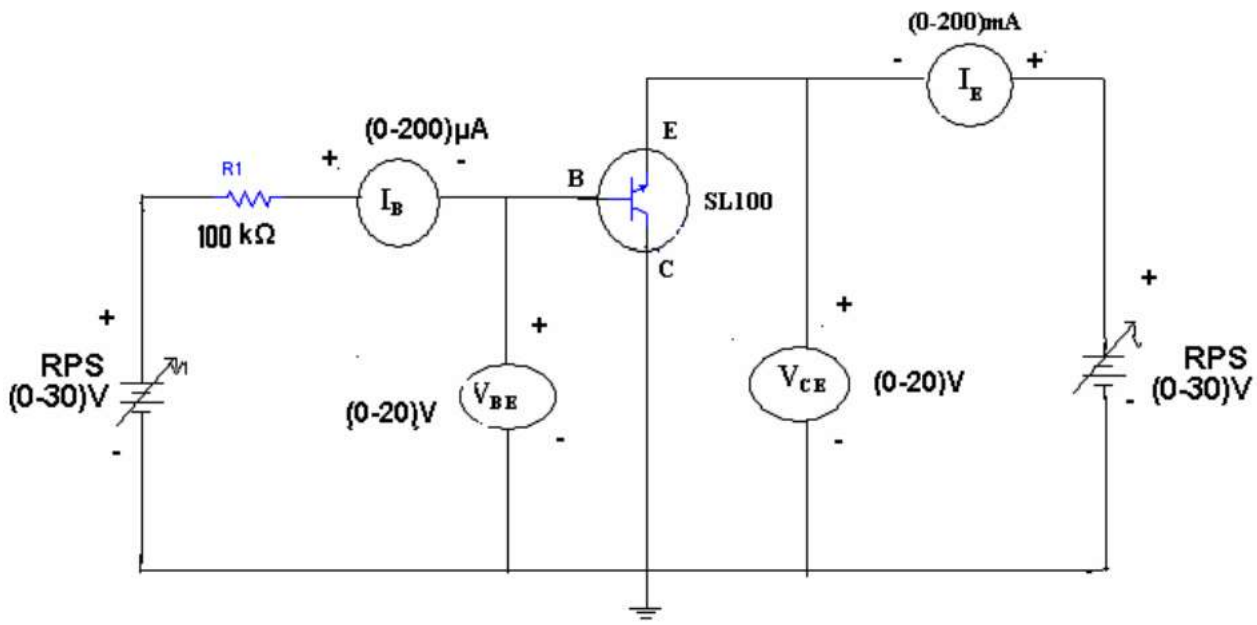$$I_B = (1 - \alpha_F) \times I_F + (1 - \alpha_R) \times I_R$$

The forward and reverse current gains are related by the expression

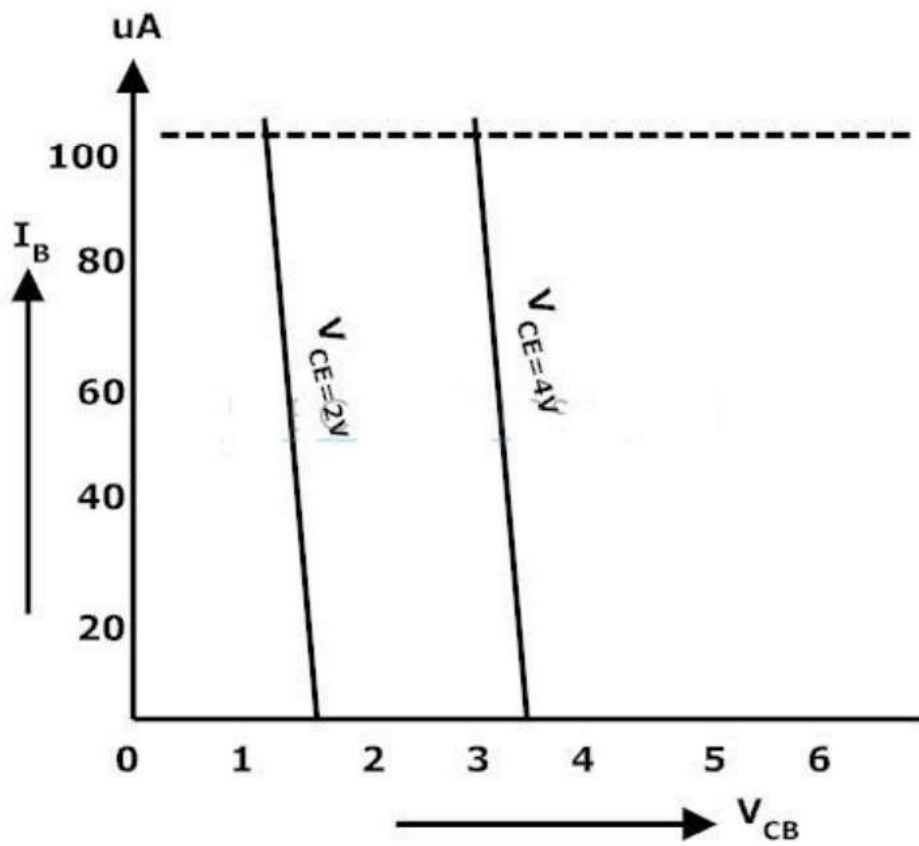$$\alpha_R \times I_{CS} = \alpha_F \times I_{ES} = I_S$$

where, I_S is the BJT transport saturation current. The parameters α_R and α_F are influenced by impurity concentrations and junction depths. The saturation current, I_S, can be expressed as
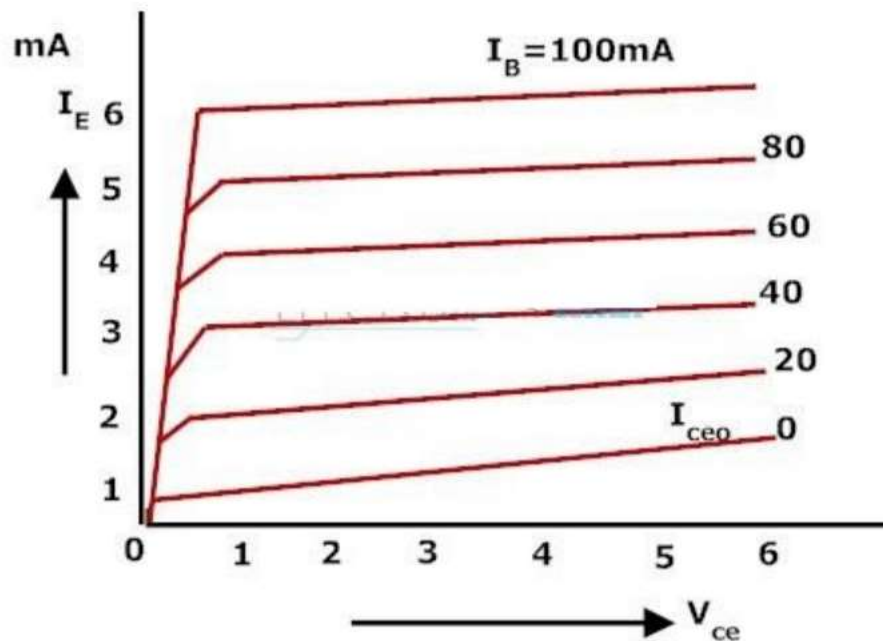
$$I_S = J_S \times A$$

where, A is the area of the emitter and J_S is the transport saturation current density.

Input Characteristic

Output Characteristic

mA

I$_E$ 6

I$_B$=100mA

5

80

4

60

40

3

20

2

I$_{ceo}$ 0

1

0   1   2   3   4   5   6

V$_{ce}$

Procedure:

Input Characteristics:

1. Connect the circuit as per the circuit diagram.

2. Set V_{CE} = 5V, vary, V_{BE} insteps of 0.1V & note down the corresponding I_B and repeat the above procedure for 10V & so on.

3. Plot the graph: V_{CB} vs I_B for a constant V_{CE}.

Output Characteristics:

1. Connect the circuit as per the circuit diagram.

2. Set I_B = 20μA, vary V_{CE} insteps of 1V & note down the corresponding I_E . Repeat the above procedure for 40μA,80μA & so on.

3. Plot the graph: V_{CE}vs I_C for a constant of I_B. .

48

Objective: To verify V-I characteristics of JFET.

Apparatus required

Power supply

Lab trainer kit

Jumper wires

Oscilloscope

Waveform generator

Multimeter

Theory

A JFET has three terminals as:

1) Source (S): The terminal through which the majority charge carriers enter the channel. Conventionally, the current entering at S is designated by I_S.

2) Drain (D): The terminal through which the majority charge carriers leave the channel. Conventionally, current entering the channel at D is designated by I_D. Drain-to-source voltage is V_{DS}.

3) Gate (G): the terminal that modulates the channel conductivity.

The JFET is a unipolar voltage controlled device. The drain current is controlled by the voltage applied at the gate. In the circuit shown self bias maintains drain current and mutual conductance g_m relatively constant. Constant g_m results a constant voltage gain. The reverse

biased junction provides high input impedance.

JFET Parameters

1. Drain Resistance (r_d): It is given by the relation of small change in drain to source voltage (V_{DS}) to the corresponding change in Drain Current (I_D) for a constant gate to source voltage (V_{GS}), when the JFET is operating in pinch-off region.

$$r_d = \Delta V_{DS}/\Delta I_D \text{ at a constant } V_{GS} \text{ (from drain characteristics)}$$

2. Trans Conductance (g_m): Ratio of small change in drain current (I_D) to the corresponding change in gate to source voltage (V_{GS}) for a constant V_{DS}.

$$g_m = \Delta I_D/\Delta V_{GS} \quad\quad\quad \text{at constant } V_{DS} \text{ (from transfer characteristics).}$$

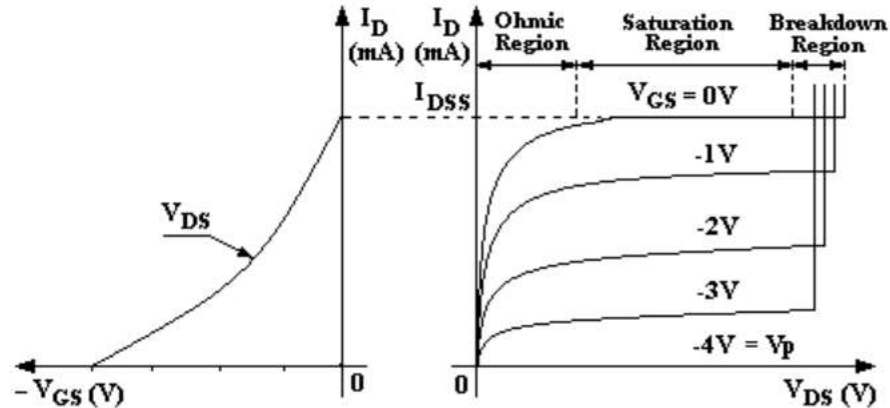The value of g_m is expressed in mho's or Siemens (s).

3. Amplification factor (μ): It is given by the ratio of small change in drain to source voltage (V_{DS}) to the corresponding change in gate to source voltage (V_{GS}) for a constant drain current (I_D).

$$\mu = (\Delta V_{DS}/\Delta I_D) \times (\Delta I_D/\Delta V_{GS}) = \Delta V_{DS}/\Delta V_{GS}$$

$$ie. \ \mu = r_d \times g_m$$

FET Transfer Characteristics   **FET Drain Characteristics**


Procedure:

Drain Characteristics:

1. Connect the circuit as shown in the figure.
2. Keep V_{GS} = 0V by varying V_{GG}.
3. Varying V_{DD} gradually in steps of 1V up to 10V note down drain current I_D and drain to source voltage (V_{DS}).
4. Repeat above procedure for V_{GS} = -0.4, -0.8, -1.2 and -1.6 V

Transfer Characteristics:

1. Connect the circuit as shown in the figure.
2. Set voltage V_{DS} = 4V/8V
3. Varying V_{DS} in steps of 0.5V until the current I_D reduces to minimum value.
4. Varying V_{GG} gradually, note down both drain current I_D and gate-source voltage (V_{GS}).
5. Repeat above procedure (step 3) for V_{DS} = 4V/ 8V
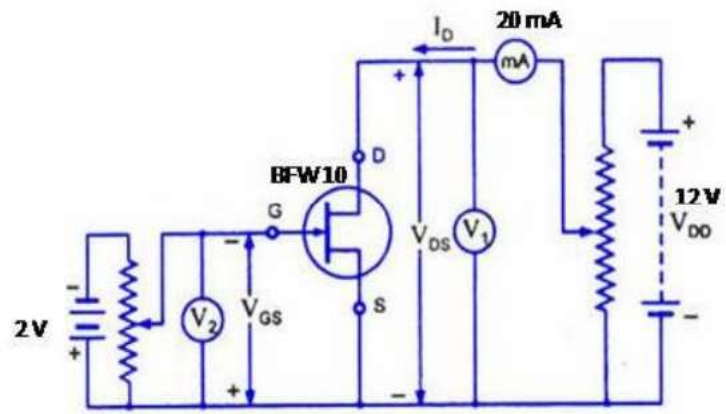
Objective: To verify V-I characteristics of MOSFET.

Apparatus required

Power supply

Lab trainer kit

Jumper wires

Oscilloscope

Waveform generator

Multimeter

Theory

MOSFET is a field effect transistor whose drain current (I_D) is controlled by the voltage on the gate. MOSFET has a much higher input impedance because of the very small gate leakage current. It has wide applications in the field of modern-era digital circuits. It is used in the amplification of the signal and switching action. Its major advantage over BJT in switching is that it is much more power efficient at high-frequency switching. It has a +ve temperature coefficient, so it is thermally stable.

MOSFET is of 2 types: a) enhancement type - n & p type b) depletion type - n & p type

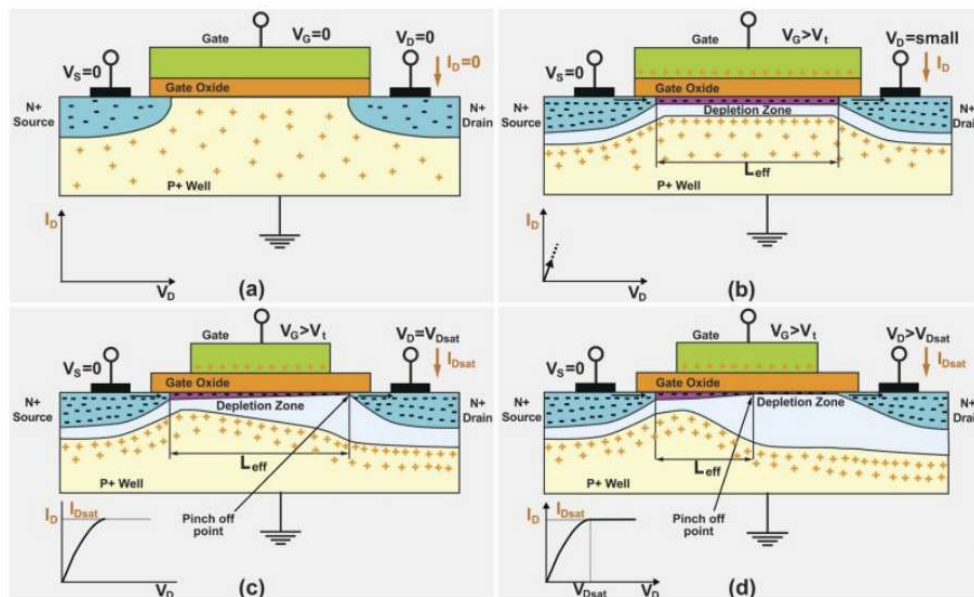The experiment will be done with n-enhancement type MOSFET.

Figure 1

Figure 1 (a) $V_G = 0$, no biasing between Gate & Source,

Figure 1(b) $V_G > V_T$, forward bias to Gate

w.r.t to Source. The -ve charge is pulled towards Gate. Thus, at a particular point number of

electrons > number of holes within the depletion region. So, there is a creation of a region

where n-type conductivity opposed to p-type is formed. This is called the inversion region.

Hence n-channel is formed through which electrons can flow.

Figure 1(c) $V_D = V_{DSat} = V_{GS} - V_T$, transition from ohmic region to saturation region,

Figure 1(d) $V_D > V_{DSat}$, pinch-off point moves towards the Source thus reducing the channel length. Under these conditions, the area between the pinch-off point and the drain is fully depleted with no inversion layer. Since this region has no positive free carriers, there is no possibility for electron-hole recombination if an electron enters the region from the electron-rich source and, if there is an electric field across the depletion zone, the electron can freely transit to the drain. The current through the device becomes controlled solely by the gate voltage under drain saturation conditions.

Circuit diagram

Nature of Graph

Transfer characteristics | Output characteristics
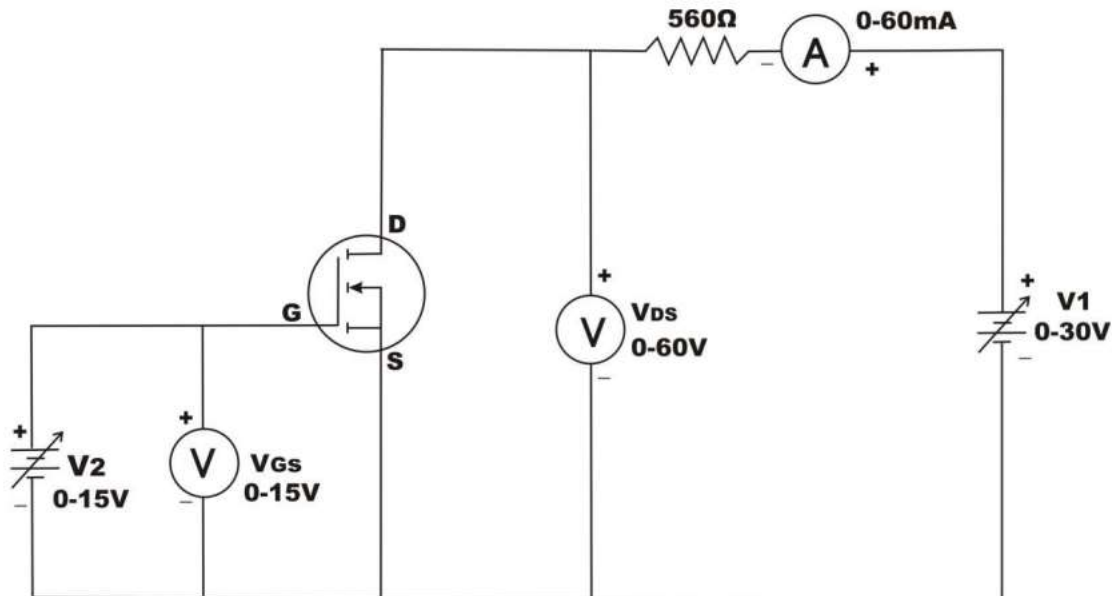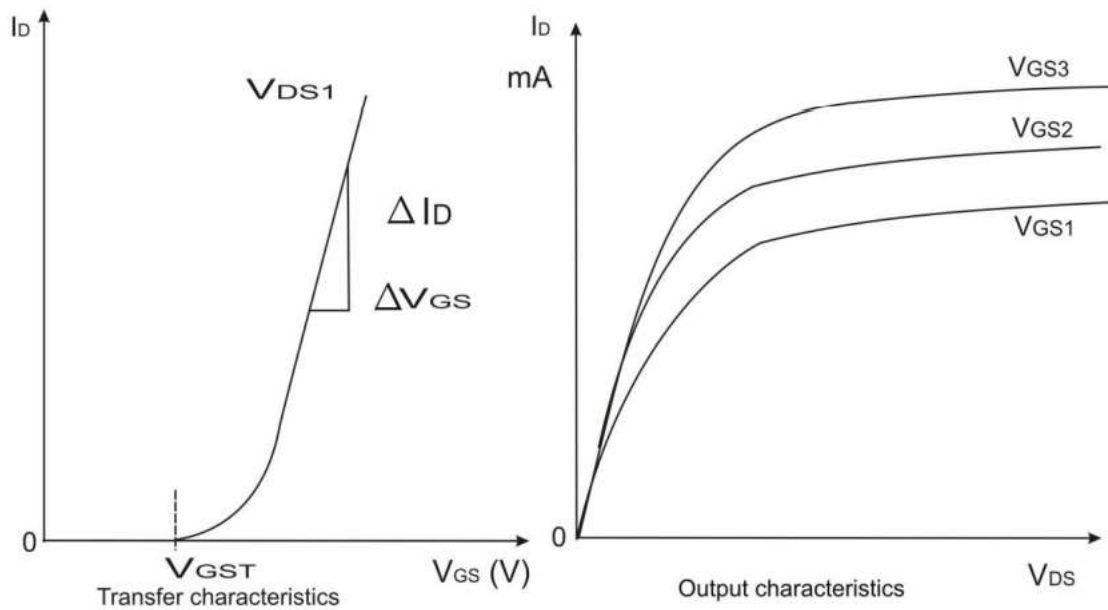
PROCEDURE:

Transfer Characteristics:

1. Make the connections as per the circuit diagram.

2. Initially keep V_1 and V_2 at 0 V.

3. Switch ON the regulated power supplies. By varying V_1, set V_{DS} to some constant voltage say 5V.

4. Vary V in steps of 0.5V, and at each step note down the corresponding values of V_{GS} and I_D. (Note: note down the value of V_{GS} at which I_D starts increasing as the threshold voltage).

5. Reduce V_1 and V_2 to zero.

6. By varying V_1, set V_{DS} to some other value say 10V.

7. Repeat step 4.

8. Plot a graph of V_{GS} versus I_D for different values of V_{DS}.

Drain or Output Characteristics:

1. Make the connections as per the circuit diagram.

2. Initially keep V_1 and V_2 at zero volts.

3. By varying V_2, set V_{GS} to some constant voltage (must be more than Threshold voltage).

4. By gradually increasing V_1, note down the corresponding value of V_{DS} and I_D. (Note: Till the MOSFET jumps to conducting state, the voltmeter which is connected across device as VDS reads approximately zero voltage. Further increase in voltage by V1 source cannot be read by VDS, so connect multimeter to measure the voltage and tabulate the readings in the tabular column).

5. Set V_{GS} to some other value (more than threshold voltage) and repeat step 4.

6. Plot a graph of V_{DS} versus I_D for different values of V_{GS}.