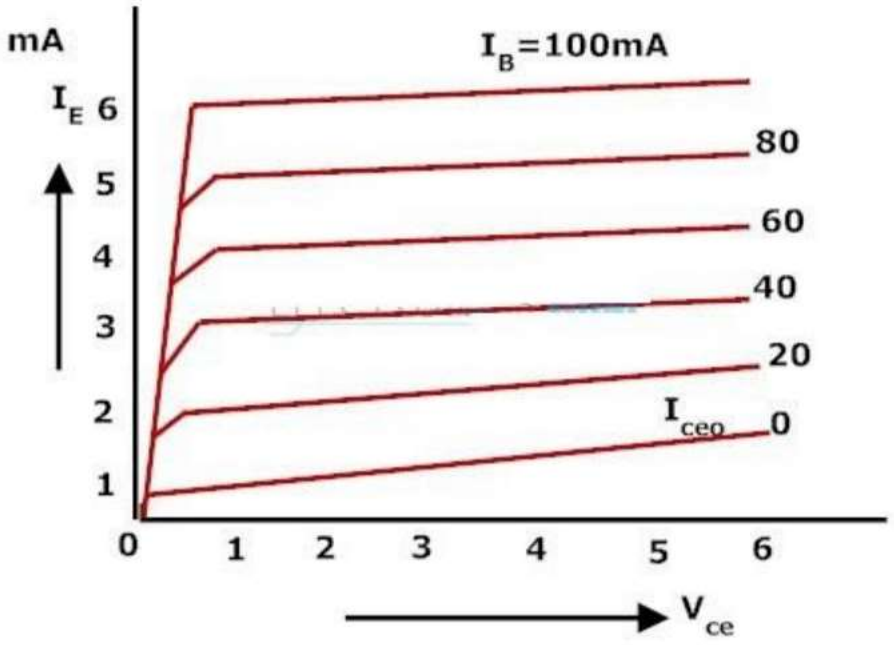
Output Characteristic



Procedure:

Input Characteristics:

1. Connect the circuit as per the circuit diagram.
2. Set V_{CE} = 5V, vary, V_{BE} insteps of 0.1V & note down the corresponding I_B and repeat the above procedure for 10V & so on.
3. Plot the graph: V_{CB} vs I_B for a constant V_{CE}.

Output Characteristics:

1. Connect the circuit as per the circuit diagram.
2. Set I_B = 20μA, vary V_{CE} insteps of 1V & note down the corresponding I_E . Repeat the above procedure for 40μA,80μA & so on.
3. Plot the graph: V_{CE}vs I_C for a constant of I_B. .

EXPERIMENT-9

Objective: To verify V-I characteristics of JFET.

Apparatus required

Power supply

Lab trainer kit

Jumper wires

Oscilloscope

Waveform generator

Multimeter

Theory

A JFET has three terminals as:

1) Source (S): The terminal through which the majority charge carriers enter the channel. Conventionally, the current entering at S is designated by I_S.

2) Drain (D): The terminal through which the majority charge carriers leave the channel. Conventionally, current entering the channel at D is designated by I_D. Drain-to-source voltage is V_{DS}.

3) Gate (G): the terminal that modulates the channel conductivity.

The JFET is a unipolar voltage controlled device. The drain current is controlled by the voltage applied at the gate. In the circuit shown self bias maintains drain current and mutual conductance g_m relatively constant. Constant $g_m$results a constant voltage gain. The reverse
biased junction provides high input impedance.

JFET Parameters

1. Drain Resistance ($\mathbf{r_d}$): It is given by the relation of small change in drain to source voltage ($\mathbf{V_{DS}}$) to the corresponding change in Drain Current ($\mathbf{I_D}$) for a constant gate to source voltage ($\mathbf{V_{GS}}$), when the JFET is operating in pinch-off region.

   $r_d = \Delta V_{DS} / \Delta I_D$ at a constant $\mathbf{V_{GS}}$ (from drain characteristics)

2. Trans Conductance ($\mathbf{g_m}$): Ratio of small change in drain current ($\mathbf{I_D}$) to the corresponding change in gate to source voltage ($\mathbf{V_{GS}}$) for a constant V_{DS}.

   $g_m = \Delta I_D / \Delta V_{GS}$ at constant $\mathbf{V_{DS}}$ (from transfer characteristics).

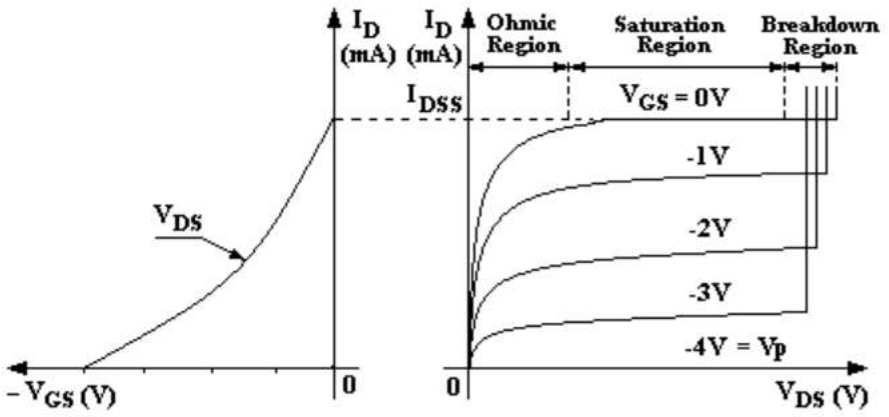
   The value of $\mathbf{g_m}$ is expressed in mho's or Siemens (s).

3. Amplification factor ($\boldsymbol{\mu}$): It is given by the ratio of small change in drain to source voltage ($\mathbf{V_{DS}}$) to the corresponding change in gate to source voltage ($\mathbf{V_{GS}}$) for a constant drain current (I_D).

$$\mu = (\Delta V_{DS}/\Delta I_D) \times (\Delta I_D/\Delta V_{GS}) = \Delta V_{DS}/\Delta V_{GS}$$

$$ie.\ \mu = r_d \times g_m$$

FET Transfer Characteristics **FET Drain Characteristics**



Procedure:

Drain Characteristics:

1. Connect the circuit as shown in the figure.
2. Keep V_{GS} = 0V by varying V_{GG}.
3. Varying V_{DD} gradually in steps of 1V up to 10V note down drain current I_D and drain to source voltage (V_{DS}).
4. Repeat above procedure for V_{GS} = -0.4, -0.8, -1.2 and -1.6 V

Transfer Characteristics:

1. Connect the circuit as shown in the figure.
2. Set voltage V_{DS} = 4V/8V
3. Varying V_{DS} in steps of 0.5V until the current I_D reduces to minimum value.
4. Varying V_{GG} gradually, note down both drain current I_D and gate-source voltage (V_{GS}).
5. Repeat above procedure (step 3) for V_{DS} = 4V/ 8V