EXPERIMENT-9

Object: -To study the flip-flop trainer.

Resources Required:

flip-flop trainer Kit, Patch Chord.

Theory:-

Basically Flip-Flops are the bistable multivibrators that stores logic 1 and logic 0.Shift registers, memory, and counters are built by using Flip – Flops. Any complex sequential machines are build using Flip – Flops. Sequential circuit (machine) output depends on the present state and input applied at that instant.

Mealy Machine is one whose output depends on both the present state and the input. Moore machines one whose output depends only on the present state of the sequential circuit. Note that the truth table of J – K Flip – Flop is same as the Master – Slave.

J – K Flip Flop and they must be remain same because IC – 7476is –ve edge trigged flip – flop and we know that race around condition is eliminated by edge triggered flip – flop. Another way of eliminating race around condition is by using Master – Slave J –K Flip – Flop. When J = K = 1 (logic HIGH), J – K Flip – Flop changes output many times for single clock pulse, it is Smaller than width of the clock pulse.
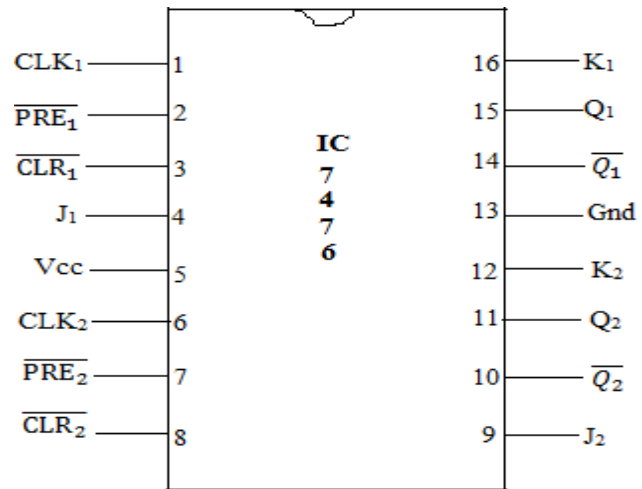
Pd < Cp = race around condition

$\qquad$ Pd $\longrightarrow$ Propagation Delay

$\quad$ CP $\qquad\longrightarrow$ Clock Pulse Width

Race around condition is eliminated by using edge triggered clock pulse and using Master – Slave J - K Flip Flops.

Implementation of J.K.Flip-Flop Design:

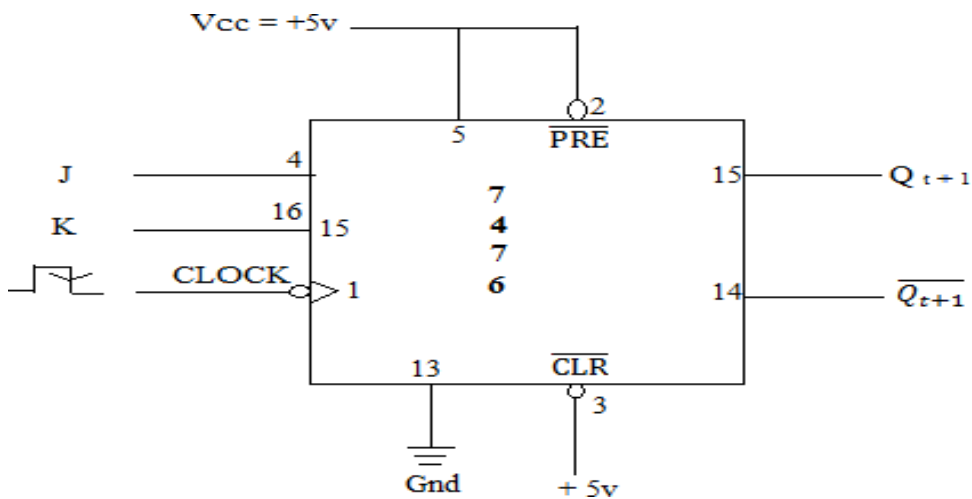**IC – 74LS76:** Dual –ve edge triggered J – K Flip – Flop
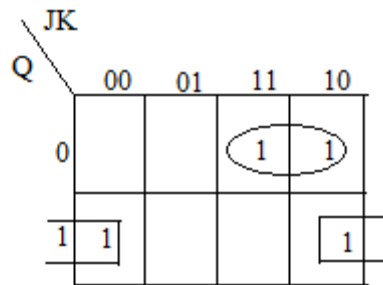**Fig Pin diagram of 7476**

Pin	Signal		Pin	Signal
1	CLK_1		16	K_1
2	$\overline{PRE_1}$		15	Q_1
3	$\overline{CLR_1}$		14	$\overline{Q_1}$
4	J_1	IC 7476	13	Gnd
5	Vcc		12	K_2
6	CLK_2		11	Q_2
7	$\overline{PRE_2}$		10	$\overline{Q_2}$
8	$\overline{CLR_2}$		9	J_2

Truth Table of JK Flip – Flop:

Inputs			Outputs
Q	J	K	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Fig J – K Flip – Flop Circuit

Where

Q   Present State

Q_{t+1} Next State
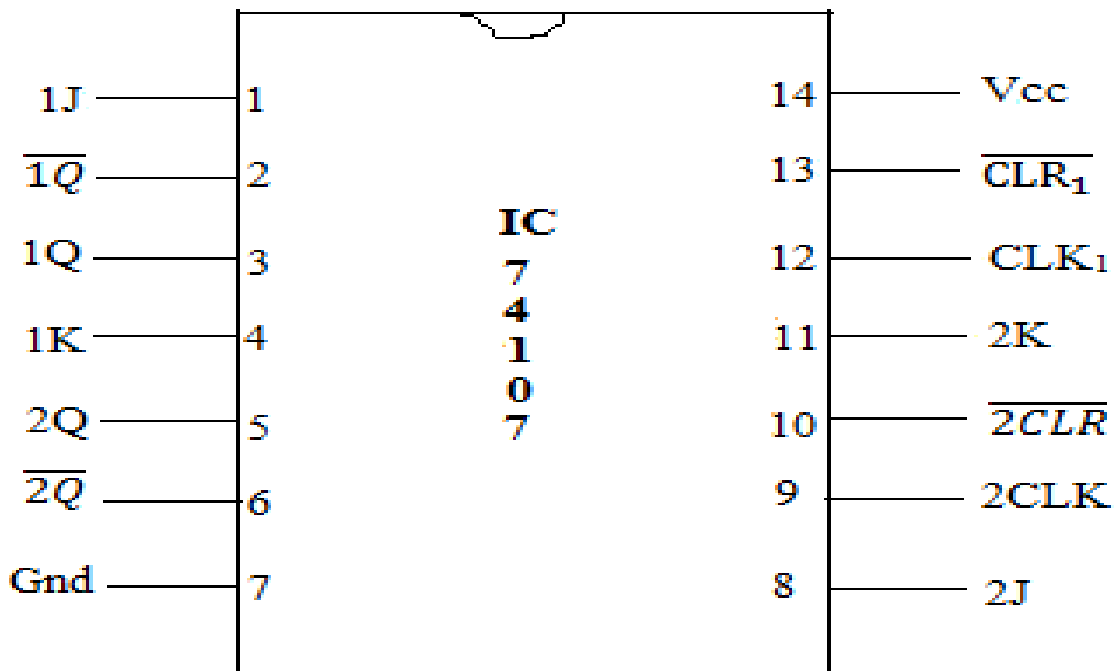

Characteristic eqn Q t + 1 = J Q + K Q

1.   Master Slave J K Flip – Flop:

IC– 74107: Dual – Master – Slave J-K Flip - Flop
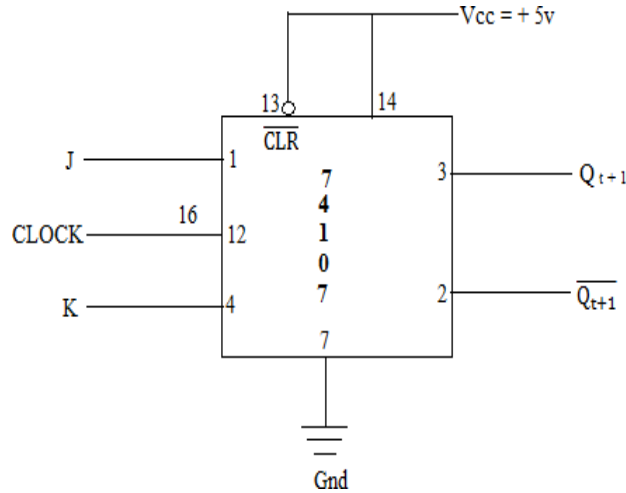
Fig Pin diagram
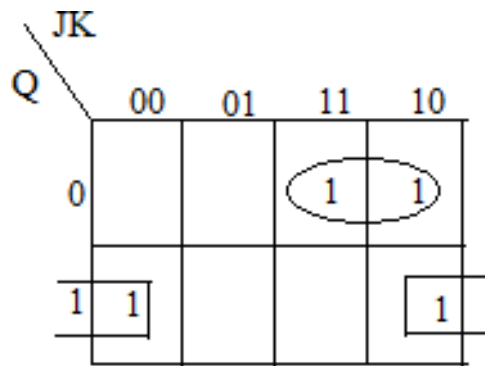
Circuit Implementation:

Fig Master – Slave J –K Flip – Flop Circuit.

Truth Table of Master – Slave – JK Flip – Flop:

where

$$Q \longrightarrow Presentstate$$
$$Q_{t+1} \longrightarrow Nextstate$$

Inputs			Outputs
Q	J	K	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Characteristic eqn $Q_{t+1}= JQ+KQ$

2. D – Flip – Flop:

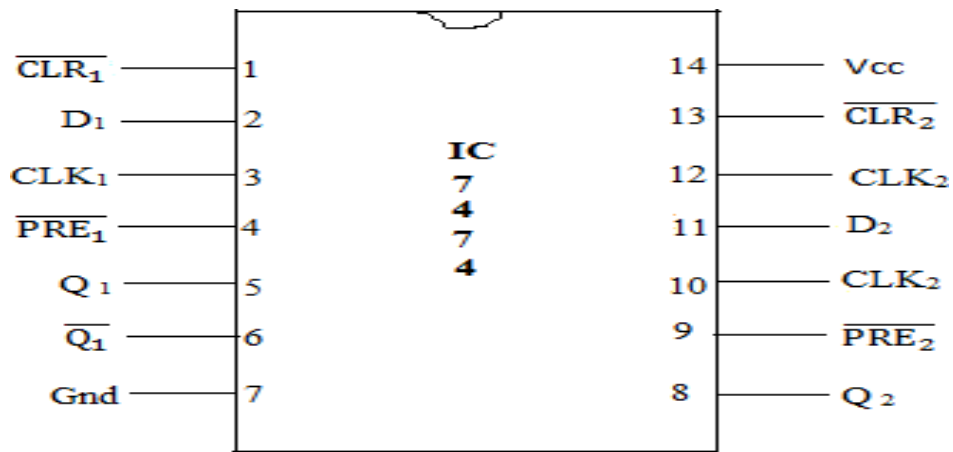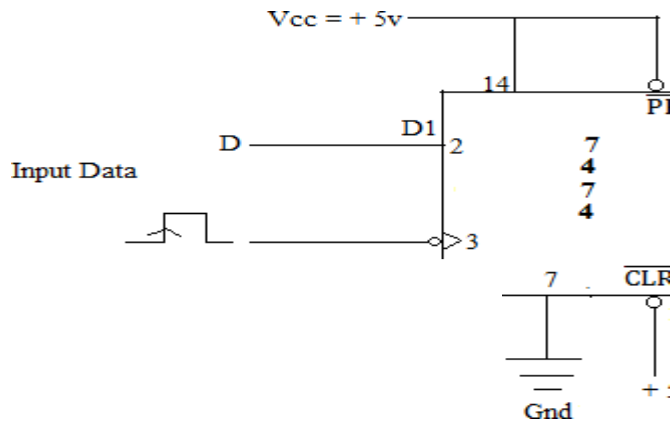**IC – 7474:** Dual + ve edge triggered D- Flip Flop :

Fig Pin Diagram

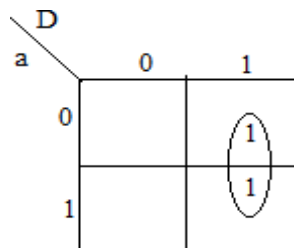**Circuit Implementation:**

Fig(8.6):D−Flip−Flop

Truth Table of D – Flip – Flop:

Where

Q $\longrightarrow$ PresentState
D $\longrightarrow$ DataInput
Q_{t+1} $\longrightarrow$ NextState

Inputs		Outputs
Q	J	Q_{t+1}
0	0	0
0	1	1
1	0	0
1	1	1

CharacteristiceqnQ_{t+1}= D

FromCharacteristic equationit isclear thatnext stateQ_{t+1}isequal tothe input data D

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i.e. $Q_{t+1}=D$

Procedure:

1) Connections are made as per the circuit diagram.
2) Apply the –ve edge triggered, +ve edge triggered and level sensitive clock pulses as required.
3) Verify the truth table of all the Flip – Flops.
4) Switch - off the power supply and disconnect the circuit.

Result: Various Flip Flop verified