EXPERIMENT-8

Objective: To design and simulate parity generator using VHDL.

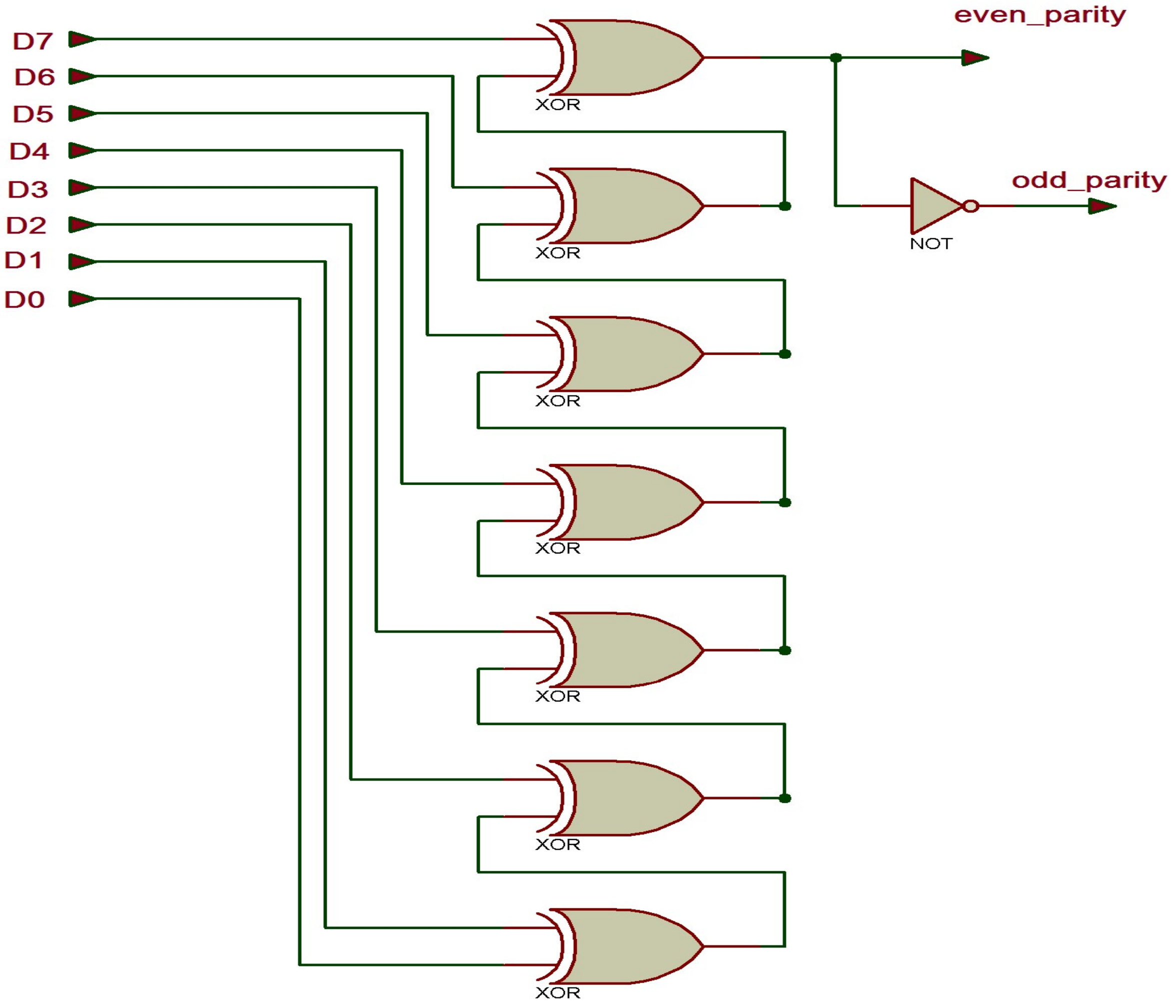
Resources Required:

Hardware Requirement: Computer

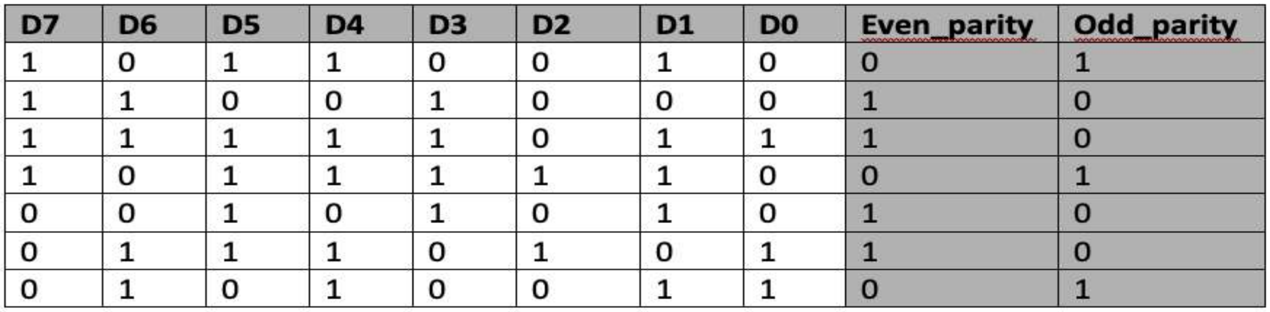
Software Requirement: XILINX 8.2 Software

Theory:

Parity evaluates whether the number of “1” bits in a binary code is odd or even. This provides a simple means of error checking. There are two types of parity with opposite results. Even parity results in a “1” if there are an odd number of “1” bits in the original code, and “0” if there are an even number. The even parity bit can be appended to the code to make the number of “1” bits even. Odd parity results in a “0” if there are an odd number of “1” bits, and “1” if there are an even number. The odd parity bit can be appended to the code to make the number of “1” bits odd.



Truth Table:

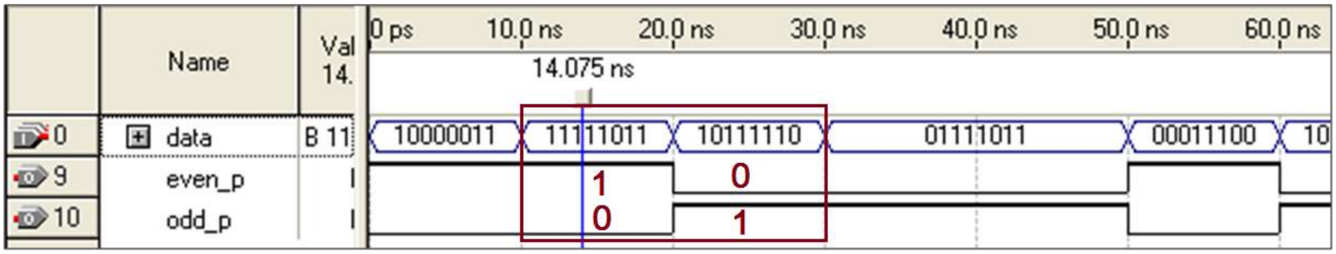


D7	D6	D5	D4	D3	D2	D1	D0	Even_parity	Odd_parity
1	0	1	1	0	0	1	0	0	1
1	1	0	0	1	0	0	0	1	0
1	1	1	1	1	0	1	1	1	0
1	0	1	1	1	1	1	0	0	1
0	0	1	0	1	0	1	0	1	0
0	1	1	1	0	1	0	1	1	0
0	1	0	1	0	0	1	1	0	1

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;
entity parity is
      port( data:in bit_vector(7 downto 0);
                  even_p,odd_p: out bit);
end parity;
architecture parity_gen of parity is
signal temp : bit_vector(5 downto 0);
  begin
    temp(0)<=data(0) xor data(1);
    temp(1)<=temp(0) xor data(2);
    temp(2)<=temp(1) xor data(3);
    temp(3)<=temp(2) xor data(4);
    temp(4)<=temp(3) xor data(5);
    temp(5)<=temp(4) xor data(6);
    even_p <= temp(5) xor data(7);
    odd_p <= not(temp(5) xor data(7));
end parity_gen;
```

Output:



Results:VHDL codes of parity generator is simulated & synthesized.