

EXPERIMENT-7

Objective: To design and simulate decoder using VHDL.

Resources Required:

Hardware Requirement: Computer

Software Requirement: XILINX 8.2 Software

Theory:

A binary decoder is a combinational logic circuit that converts a binary integer value to an associated pattern of output bits. They are used in a wide variety of applications, including data de- multiplexing, seven segment display, and memory address decoding. Decoder is with multiple data inputs and multiple outputs that convert every unique combination of data input states into a specific combination of output states.

Example: Imagine you are a mall security guard. In your office is a very important and unique public announcement (PA) phone. The phone has three dialing buttons (A, B, C) and is connected to eight different speakers, as shown in Table 1. Consequently, you get to choose which section of the mall hears your announcement based on the set of buttons you press. For example, if you press A and B and start speaking into the phone (ABC = 110), the Food Court (D6) is the only place that can hear you. However, if you press A and C (ABC = 101) then the Lady’s Room (D5) is the only place that can hear you.

Such a public announcement phone (or PA system) is an example of a 3-to-8 decoder. Since the phone has three buttons each of which can either be in one of two possible states — pressed (=1) or not pressed (= 0) — then the phone can dial eight possible different numbers ($2^3 = 2*2*2 = 8$) as shown below

A	B	C	MALL AREA
0	0	0	Security lunch room (D0)
0	0	1	Men's Room (D1)
0	1	0	Footwear Stores (D2)
0	1	1	Jewelry Dealers (D3)
1	0	0	Appliance Stores (D4)

1	0	1	Lady's Room (D5)
1	1	0	Food Court (D6)
1	1	1	Bookstores (D7)

Truth Table:

Inputs				Outputs							
EN	A	B	C	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Boolean Expression

$$Y_0 = A'B'C'$$

$$Y_1 = A'B'C$$

$$Y_2 = A'BC'$$

$$Y_3 = A'BC$$

$$Y_4 = AB'C'$$

$$Y_5 = AB'C$$

$$Y_6 = ABC'$$

$$Y_7 = ABC$$

Application: The Decoders were used in analog to digital conversion in analog decoders, Used in electronic circuits to convert instructions into CPU control signals, also used in logical circuits, data transfer.

VHDL Code:

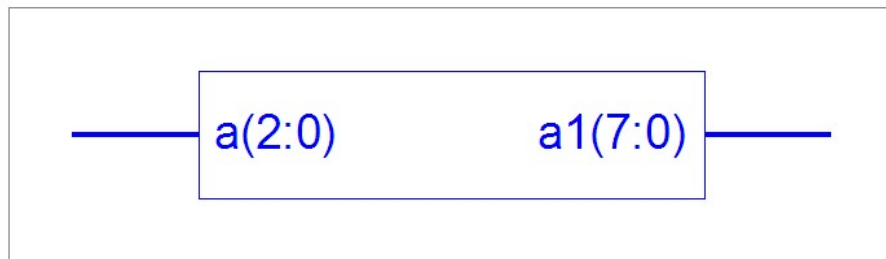
Behavioral Modelling

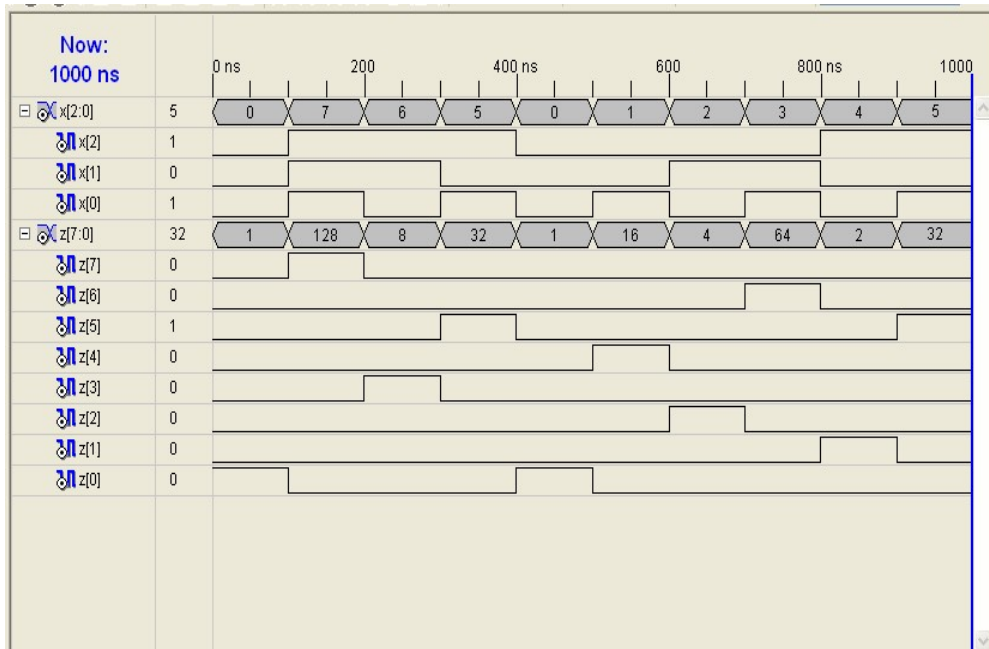
```
entity decoder is
Port ( a : in  STD_LOGIC_VECTOR(2 DOWNTO 0);
      a1 : out STD_LOGIC_VECTOR(7 DOWNTO 0));
end decoder;
```

```
architecture Behavioral of decoder is
begin
process(a)
begin
case a is
when "000"=>a1<="10000000";
when "001"=>a1<="01000000";
when "010"=>a1<="00100000";
when "011"=>a1<="00010000";
when "100"=>a1<="00001000";
when "101"=>a1<="00000100";
when "110"=>a1<="00000010";
when "111"=>a1<="00000001";
when others=>>null;
end case;
end process;
end Behavioral;
```

Output:

RTL Schematic:





Results: VHDL codes of 3:8 decoder is simulated & synthesized