EXPERIMENT-6

Objective: To design and simulate encoder using VHDL.

Resources Required:

Hardware Requirement: Computer

Software Requirement: XILINX 8.2 Software

Theory:

An encoder is a digital circuit that converts a set of binary inputs into a unique binary code. The binary code represents the position of the input and is used to identify the specific input that is active. Encoders are commonly used in digital systems to convert a parallel set of inputs into a serial code. The 8 to 3 Encoder or octal to Binary encoder consists of 8 inputs: d7 to d0 and 3 outputs: a2, a1 & a0. Each input line corresponds to each octal digit and three outputs generate corresponding binary code. The figure below shows the logic symbol of octal to the binary encoder.

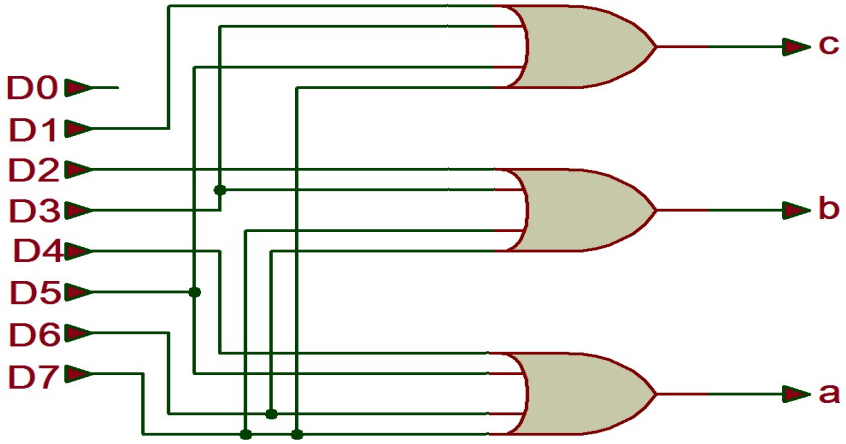


Figure 6.1 : Logical Diagram of 8:3 encoder

Truth Table:

INPUTS								OUTPUTS		
d7	d6	d5	d4	d3	d2	d1	d0	a(2)	a(1)	a(0)
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

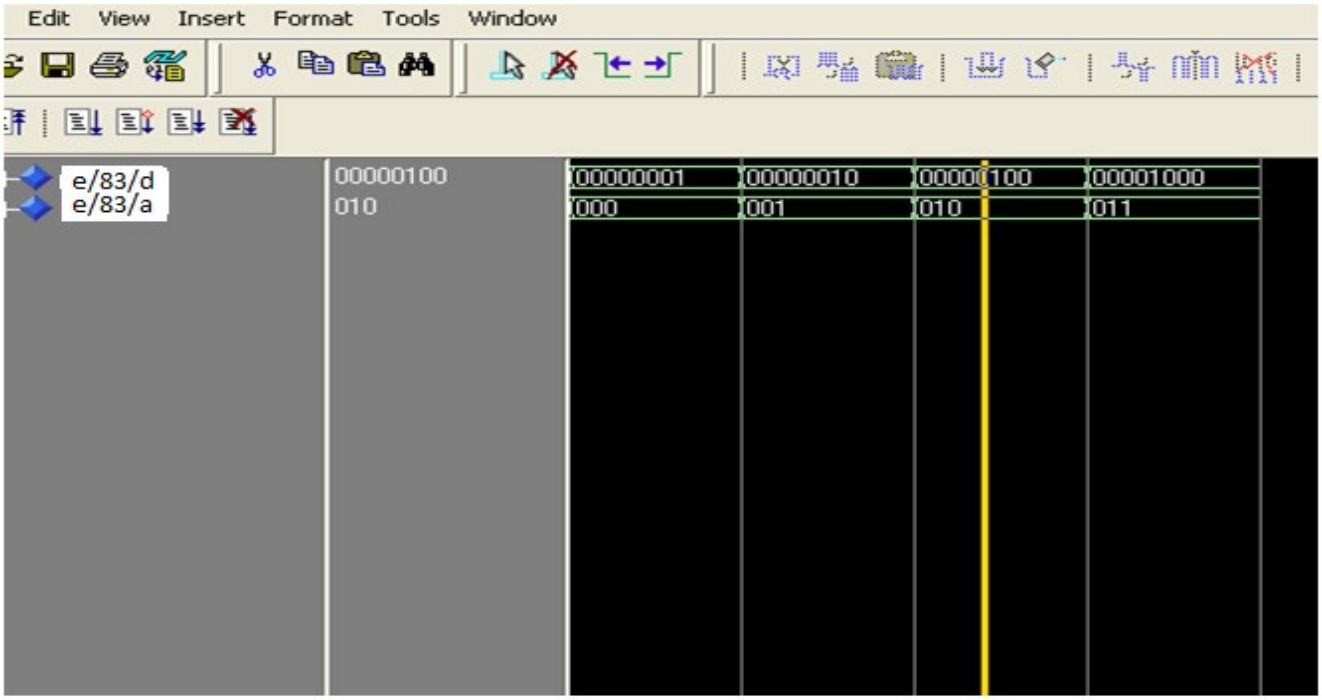
VHDL Code:

Behavioral Modelling

```
library ieee;
use ieee.std_logic_1164.all;
entity encoder83 is
port(d: in std_logic_vector(7 downto 0);
     a: out std_logic_vector(2 downto 0));
end encoder83;
architecture behavioral of encoder83 is
begin
process(d)
begin case d is
when "00000001"=> a<="000";    when "00000010"=> a<="001";
when "00000100"=> a<="010";    when "00001000"=> a<="011";
when "00010000"=> a<="100";    when "00100000"=> a<="101";
when "01000000"=> a<="110";    when "10000000"=> a<="111";
when others=> a<="UUU";  end case; end process;
end behavioral;
```

Output:

RTL Schematic:



Results: VHDL codes of 8:3 encoder is simulated & synthesized