EXPERIMENT- 5

Objective: To design and simulate demultiplexer using VHDL.

Resources Required:

Hardware Requirement: Computer

Software Requirement: XILINX 8.2 Software

Theory:

A digital combinational circuit which takes one input signal and generates multiple output signals is known as demultiplexer or DEMUX. As it distributes a single input signal over many output lines, hence it is also referred to as a type of data distributor.

In a demultiplexer, there is only 1 input line and 2^n output lines. Where, n denotes the number of select lines. Therefore, it can be noted that a demultiplexer reverses the operation of a multiplexer. In 1 to 8 demultiplexer, there are total of eight outputs, i.e., Y0, Y1, Y2, Y3, Y4, Y5, Y6, and Y7, 3 selection lines, i.e., S0, S1and S2 and single input, i.e., a. On the basis of the combination of inputs which are present at the selection lines S0, S1 and S2, the input will be connected to one of these outputs.

Truth Table:

DATA INPUT	SELECT INPUTS			OUTPUTS							
a	S2	S1	S0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
a	0	0	0	a	0	0	0	0	0	0	0
a	0	0	1	0	a	0	0	0	0	0	0
a	0	1	0	0	0	a	0	0	0	0	0
a	0	1	1	0	0	0	a	0	0	0	0
a	1	0	0	0	0	0	0	a	0	0	0
a	1	0	1	0	0	0	0	0	a	0	0
a	1	1	0	0	0	0	0	0	0	a	0
a	1	1	1	0	0	0	0	0	0	0	a

Applications of Demultiplexers: Digital demultiplexers are combinational devices controlled by a selector address that routes input data to one of many outputs of the demultiplexers. These can be used in data demultiplexing, clock demultiplexing, memory addressing, four phase clock generator, function generation using DMUX, switch encoding, serial to parallel converter.

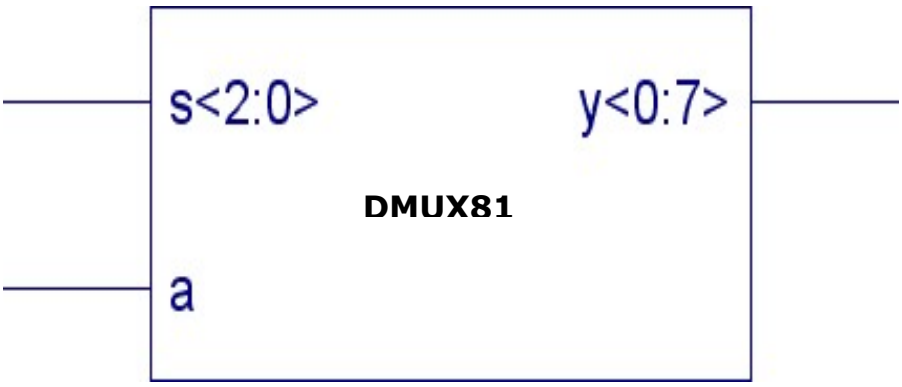
VHDL Code:

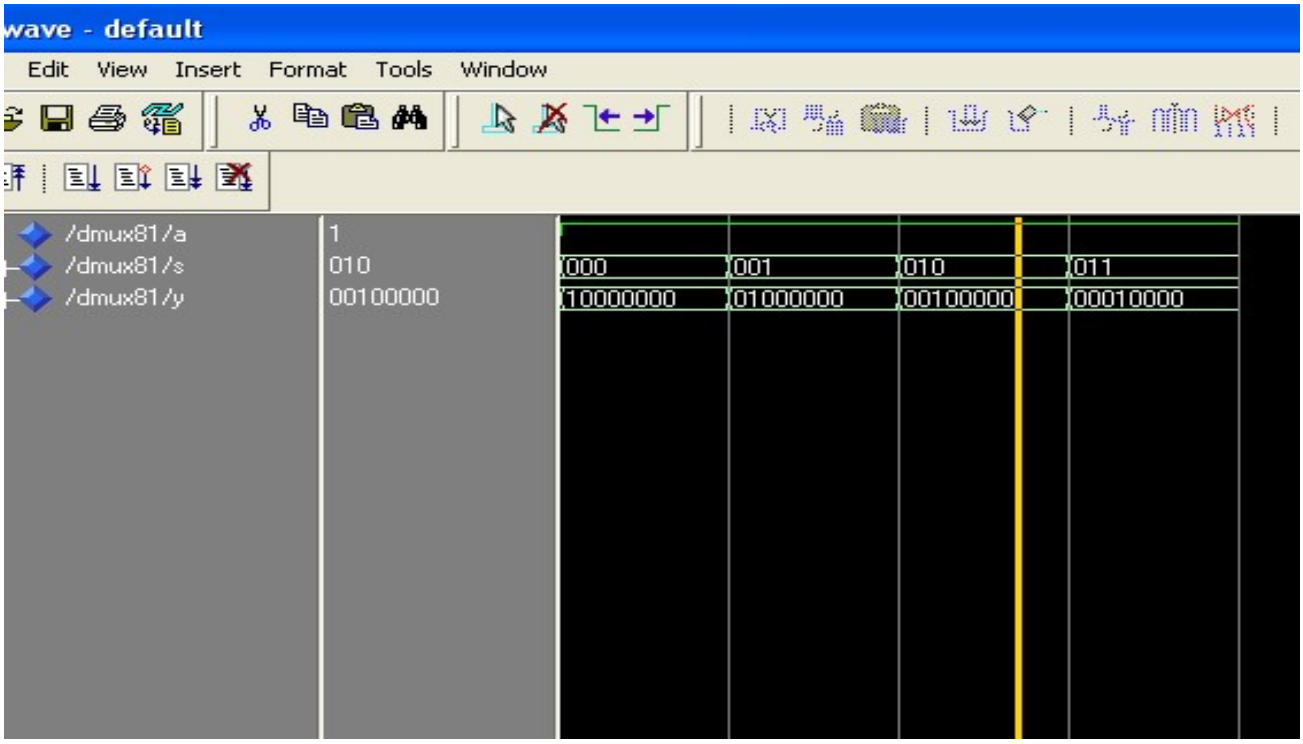
```
use ieee.std_logic_1164.all;
entity dmux81 is
port(a: in std_logic;s: in std_logic_vector(2 downto 0);
```

```
     y: out std_logic_vector(0 to 7));
end dmux81;
architecture dmux of dmux81 is
begin
process(a,s)
begin y<="00000000";
case s is
when "000"=> y(0)<=a;     when "001"=> y(1)<=a;    when "010"=> y(2)<=a;
when "011"=> y(3)<=a;     when "100"=> y(4)<=a;    when "101"=> y(5)<=a;
when "110"=> y(6)<=a;     when "111"=> y(7)<=a;
when others=> y<="UUUUUUUU";
end case; end process;
end dmux;
```

Output:

RTL Schematic





Results:VHDL codes of 1:8 demultiplexer is simulated & synthesized.