Objective: To design and simulate multiplexer using VHDL.

Resources Required:

Hardware Requirement: Computer

Software Requirement: XILINX 8.2 Software

Theory:

Multiplexer is simply a data selector. It has multiple inputs and one output. Any one of the input line is transferred to output depending on the control signal. This type of operation is usually referred as multiplexing. In 8:1 multiplexer, there are 8 inputs. Any of these inputs are transferring to output, which depends on the control signal. For 8 inputs we need 3 bit wide control signal. If control signal is "000" then the fist input is transferring to output line. If thee control signal is "111" then the last input is transferring to output. Similarly, for all values of control signals.
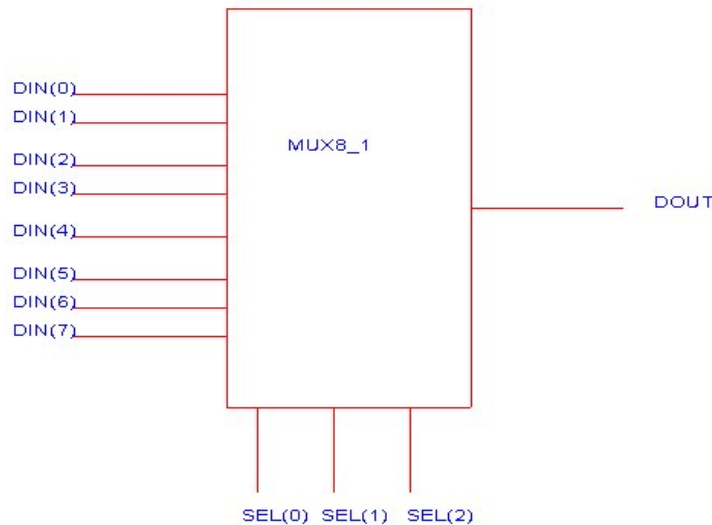

Figure 4.1 : Logical Diagram of 8:1 Mux

Truth Table:

Data Input	Select Inputs			Outputs							
D	S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0

Simplified as:

Select Data Inputs			Output
S_2	S_1	S_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

Boolean Expression

$$Y = D0\ \overline{S2}\ \overline{S1}\ \overline{S0} + D1\ \overline{S2}\ \overline{S1}\ S0 + D2\ \overline{S2}\ S1\ \overline{S0} + D3\ \overline{S2}\ S1\ S0 + D4\ S2\ \overline{S1}\ \overline{S0} + D5\ S2\ \overline{S1}\ S0$$
$$+ D6\ S2\ S1\ \overline{S0} + D7\ S2\ S1\ S0$$

Application: Communication systems for modulation purpose, telephone networks, parallel to serial convertor.

VHDL Code:

```
Behavioral Modelling
entity mux is
Port (s : in  STD_LOGIC_VECTOR (2 downto 0);
x : in  STD_LOGIC_VECTOR (7 downto 0);
y : out  STD_LOGIC);
end mux;

architectureBehavioral of mux is
begin
process(s,x)
begin
if s="000" then y<=x(0);
elsif s="001" then y<=x(1);
elsif s="010" then y<=x(2);
elsif s="011" then y<=x(3);
elsif s="100" then y<=x(4);
elsif s="101" then y<=x(5);
elsif s="110" then y<=x(6);
elsif s="111" then y<=x(7);
```
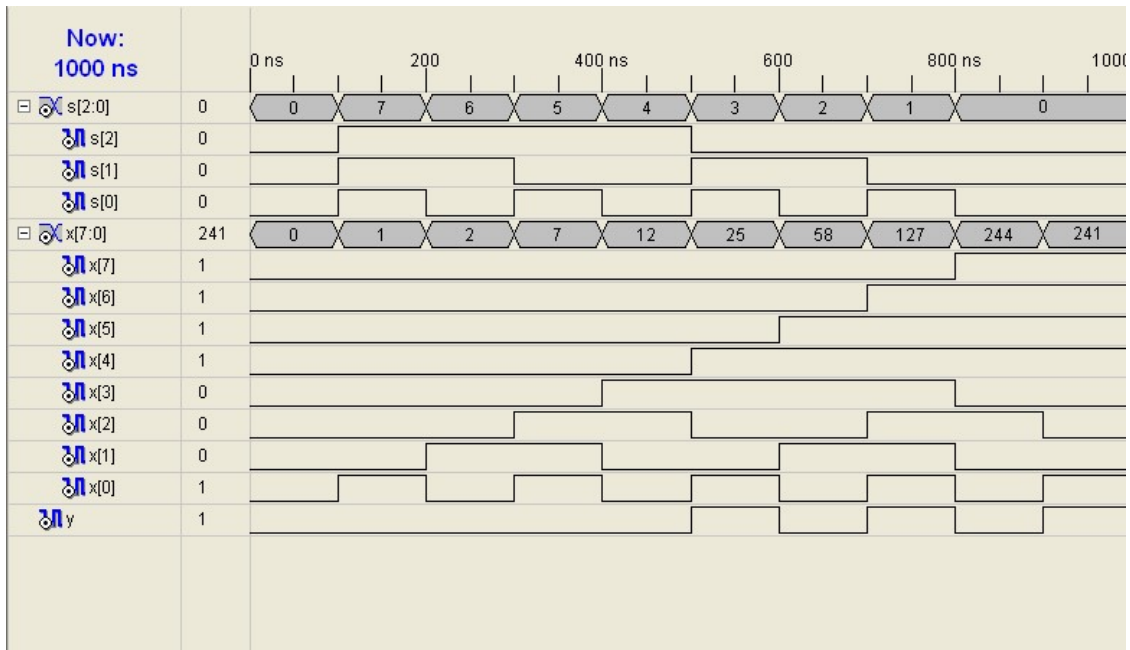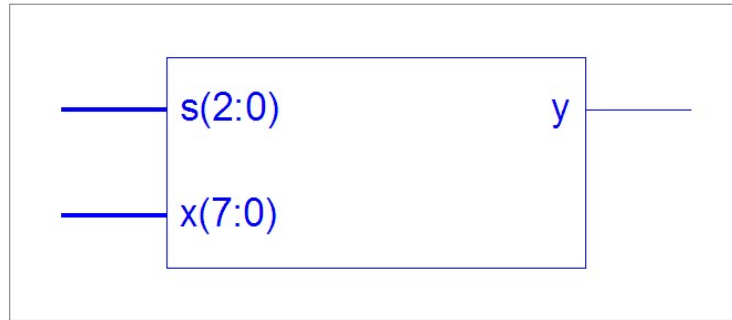
```
end if;
end process;
end Behavioral;
```

Output:

RTL Schematic

Results: VHDL codes of 8:1 Multiplexer is simulated & synthesized.