EXPERIMENT-3

Objective: To design and simulate full adder using VHDL.

Resources Required:

Hardware Requirement: Computer

Software Requirement: XILINX 8.2 Software

Theory:

Full adder is the adder which adds three inputs and produces two outputs. The first two inputs are **a** and **b** and the third input is an input carry as **c**. The output carry is designated as **cy** and the normal output is designated as **s** which is SUM.

Truth Table:

INPUTS			OUTPUTS	
a	b	c	s	cy
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean Expression

```
s = (a xor b)xor c;
cy = (a and b) or (b and c) or (c and a);
```

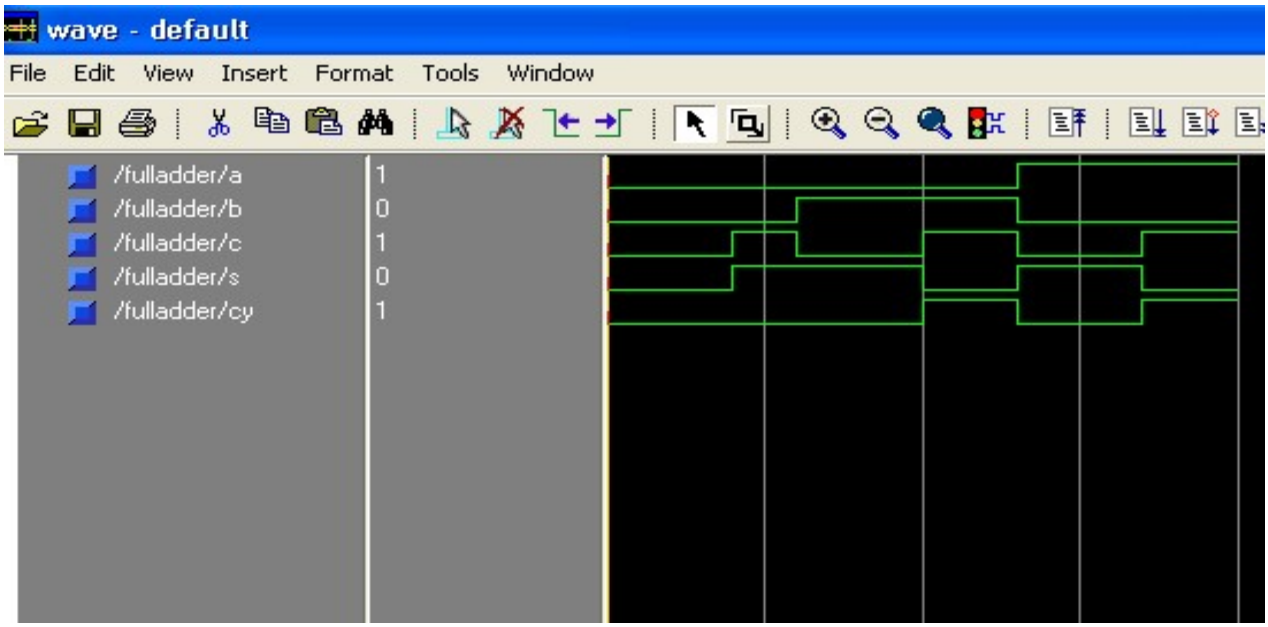
VHDL Code:

```
Dataflow Modelling
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;
     --Entity Declarations
entity fulladder is
port(a,b,c: in std_logic;
     s,cy: out std_logic);
end fulladder;
```

```
architecture dataflow of fulladder is
begin
s<= (a xor b)xor c;
cy<= (a and b) or (b and c) or (c and a);
end dataflow;
```

Output:

RTL Schematic



Results: VHDL codes of full adder is simulated & synthesized