EXPERIMENT-2

Objective: To design and simulate half adder using VHDL.

Resources Required:

Hardware Requirement: Computer

Software Requirement: XILINX 8.2 Software

Theory:

Half adders' primary function is to add two bits or two digits, so the input port has two variables, **a** and **b** which corresponds to the digits/numbers that have to be added. The result of adding two bits/digits is the **sum (s)** and the **carryout (c)** which corresponds to the outputs ports.

Truth Table:

INPUTS		OUTPUTS	
a	b	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Boolean Expression

s= a xor b;

c = a and b;

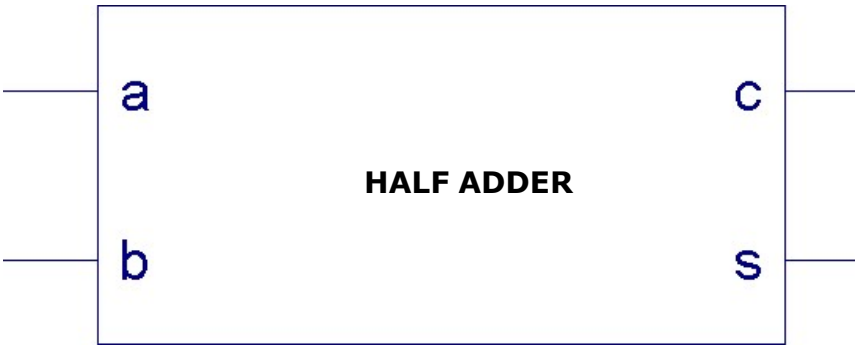
VHDL Code:

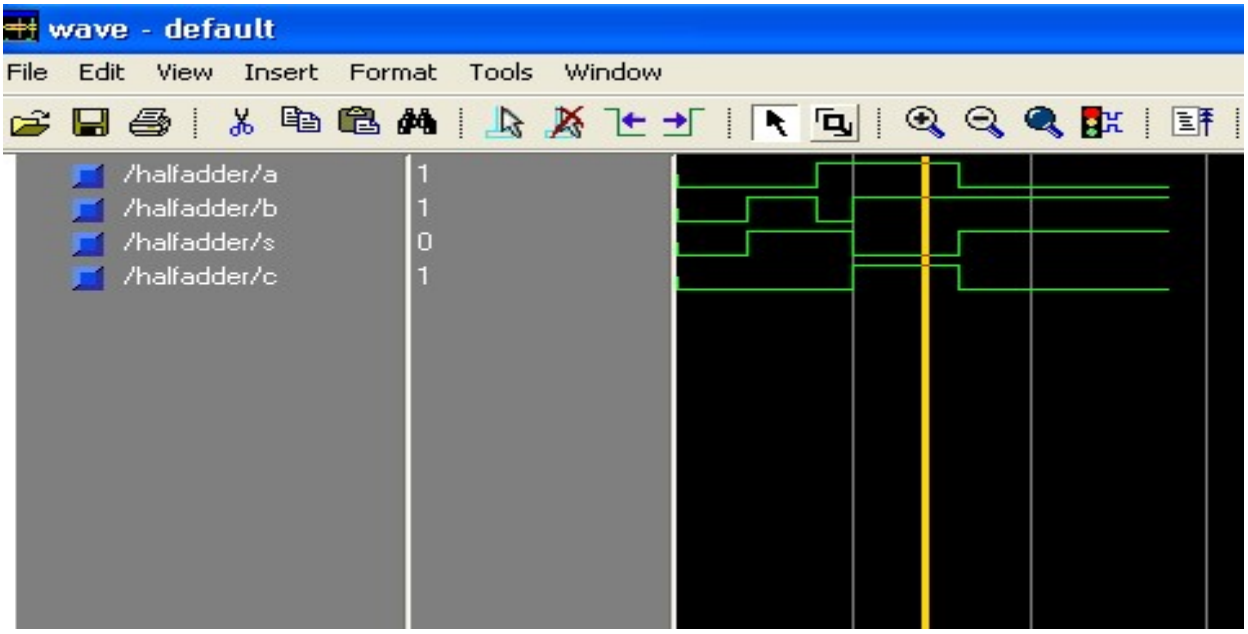
```
Dataflow Modelling
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;
     --Entity Declarations
entity halfadder is
port(a,b: in std_logic;
     s,c: out std_logic);
end halfadder;
architecture dataflow of halfadder is
begin
```

```
s<= a xor b;
c<= a and b;
end dataflow;
```

Output:

RTL Schematic





Results: VHDL codes of half adder is simulated & synthesized