EXPERIMENT- 1

Objective: To study the single stage RC coupled CE, CB, CC amplifier.

Resources Required: Transistor, Resistance , Regulated Power supply, Capacitor, Signal Generator, CRO , Breadboard and Wires ,CRO Probes

Thoery:

The single stage common emitter amplifier circuit shown below uses what is commonly called "Voltage Divider Biasing" or “self biasing”. The Common Emitter Amplifier circuit has a resistor in its Collector circuit. The current flowing through this resistor produces the voltage output of the amplifier. The value of this resistor is chosen so that at the amplifiers quiescent operating point, Q-point this output voltage lies half way along the transistors load line. In Common Emitter Amplifier circuits, capacitors C1 and C2 are used as Coupling Capacitors to separate the AC signals from the DC biasing voltage. This ensures that the bias condition set up for the circuit to operate correctly is not affected by any additional amplifier stages, as the capacitors will only pass AC signals and block any DC component.

The output AC signal is then superimposed on the biasing of the following stages. Also a bypass capacitor, CE is included in the Emitter leg circuit. This capacitor is an open circuit component for DC bias meaning that the biasing currents and voltages are not affected by the addition of the capacitor maintaining a good Q-point stability. However, this bypass capacitor short circuits the Emitter resistor at high frequency signals and only RL plus a very small internal resistance acts as the transistors load increasing the voltage gain to its maximum.

Generally, the value of the bypass capacitor, CE is chosen to provide a reactance of at most, 1/10th the value of RE at the lowest operating signal frequency.

Circuit Diagram:

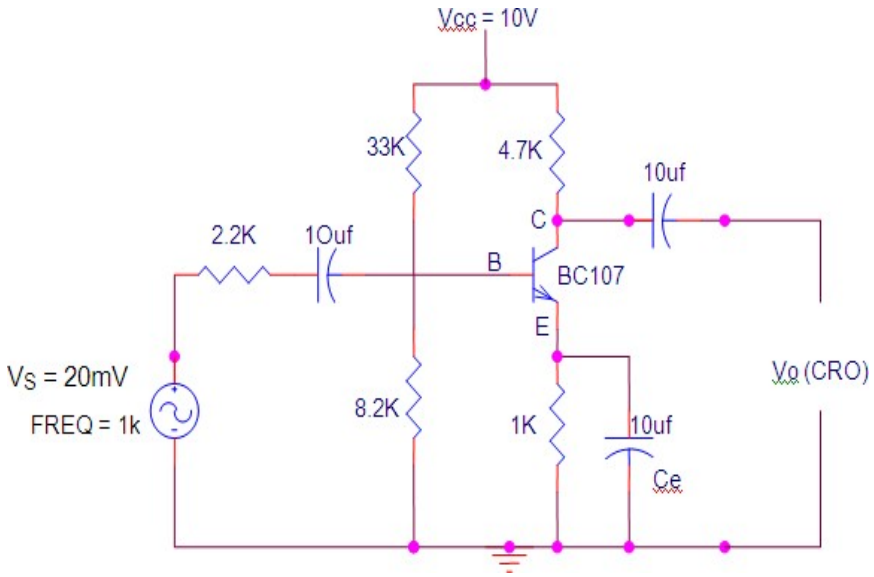

Fig: CE Amplifier Circuit

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. A 10V supply is given to the circuit.
3. A certain amplitude of input signal (say 20mv at 1 kHz) is kept constant using signal generator and for different frequencies, the output voltage (V0) from CRO are noted.
4. Gain for with and without feedback is calculated using Gain (in dB)= 20 log (V_0/V_i) where Vo is output voltage, Vi is input voltage.
5. Plot the graph between Gain (in dB) and frequency
6. Repeat the circuit diagram shown above for CB and CC configuration.

Model graph:

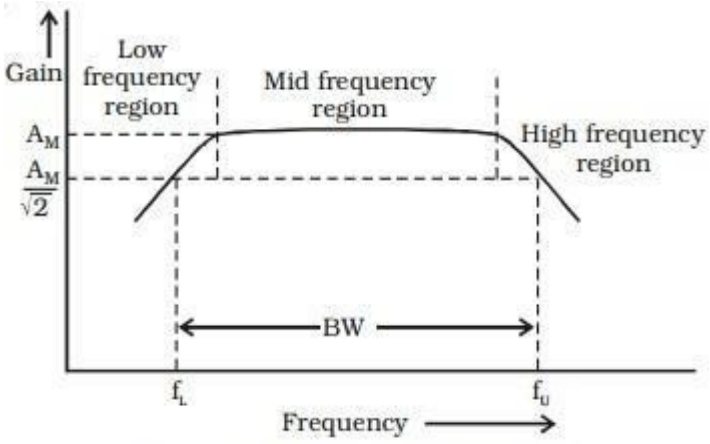

Fig Frequency response curve

OBSERVATION TABLE:

S.No	Frequency(hz)	Output voltage(vo)	Voltage gain (vo/vi)	Gain (db) Avf=20 log (vo/vi).

Bandwidth of the CE amplifier = fh-fl HZ

PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.
3. Make sure while selecting the emitter, base and collector terminals of the transistor.

RESULT: The Frequency response characteristics of Common emitter amplifier are obtained and the graph was plotted. From the graph, the Bandwidth was obtained as ……..